

Figure 1

# Macro-Cell basic architecture

## Macro-Cell Configuration and Control

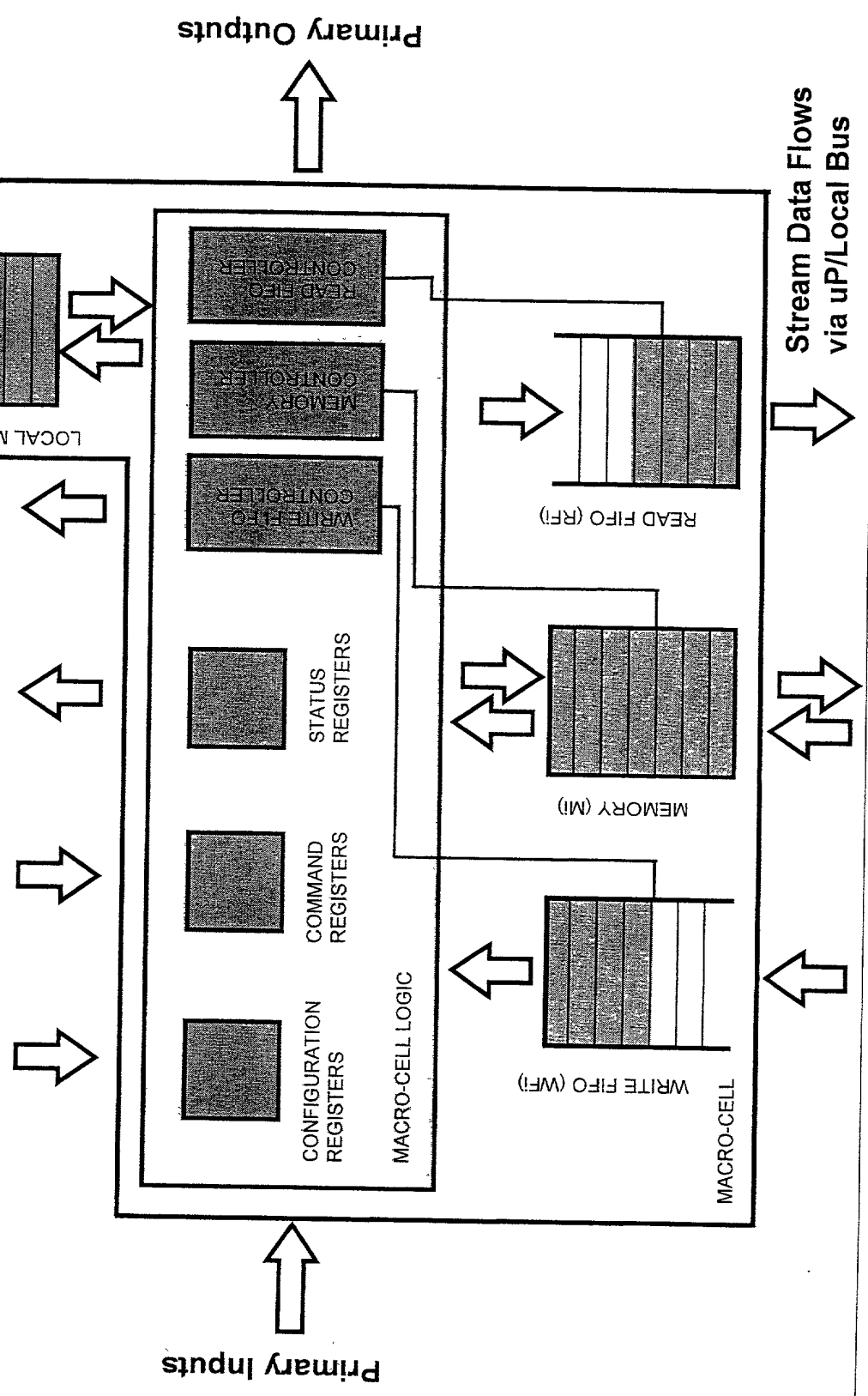
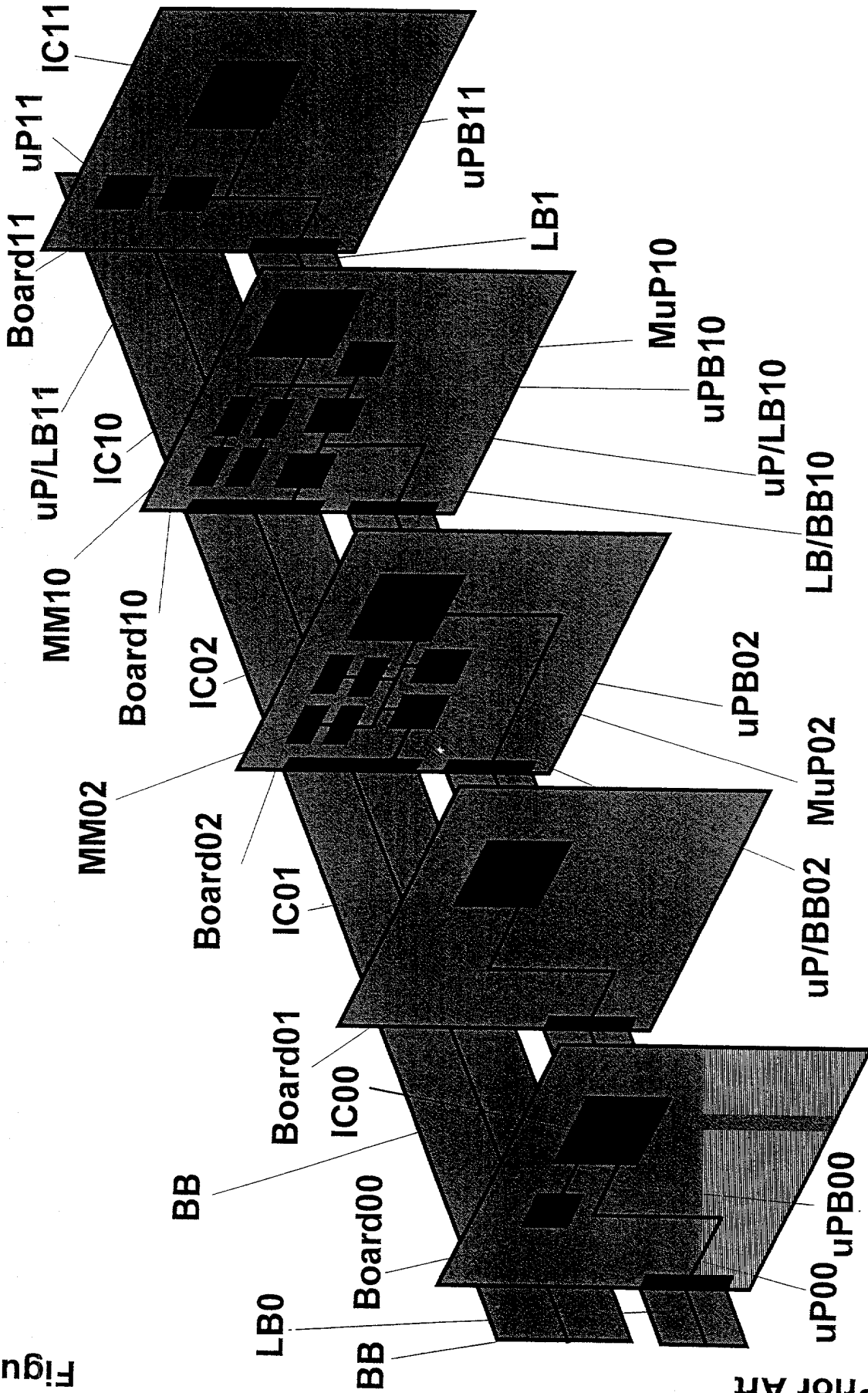


Figure 1

Prior Art

Figure 2

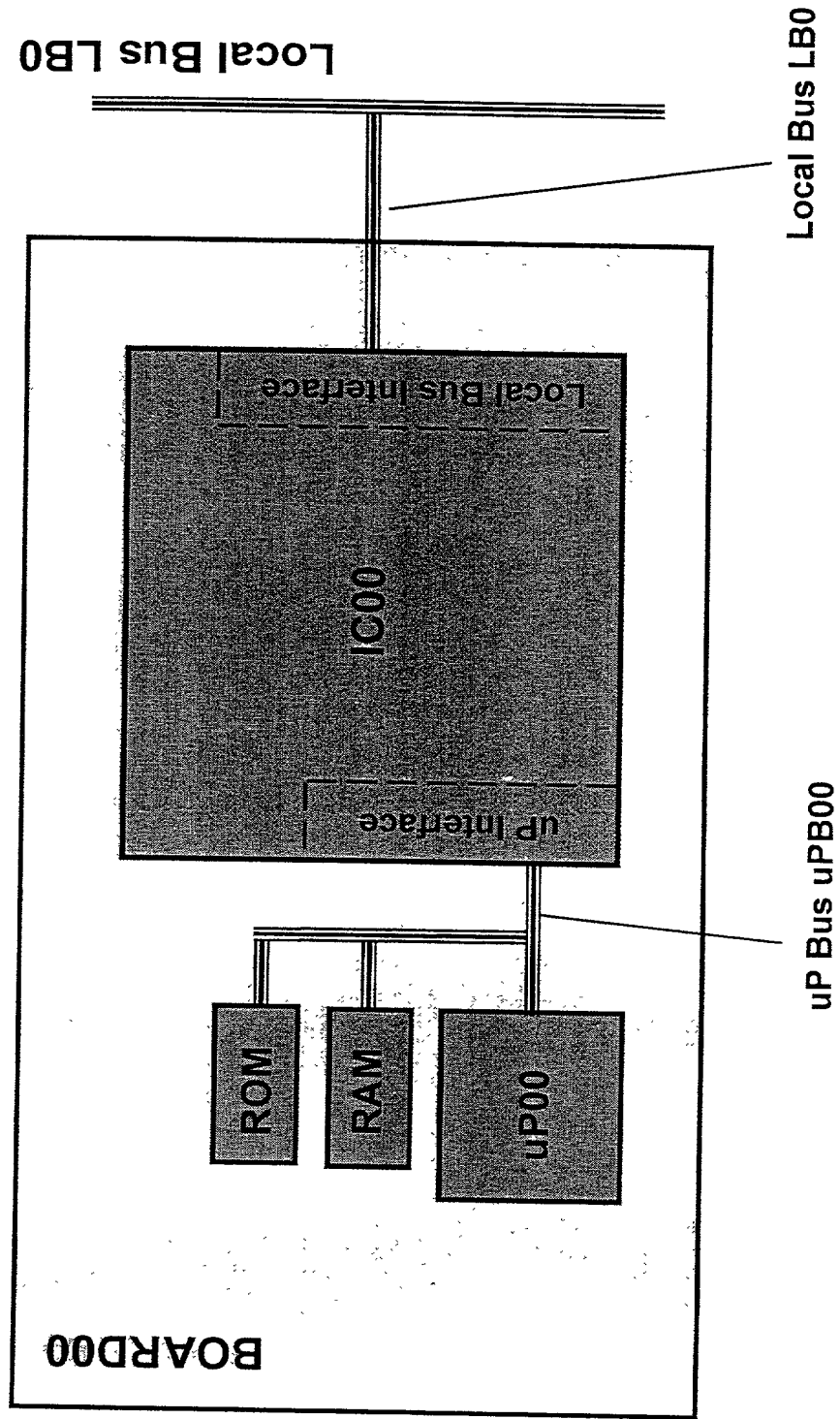
# BUS BASED MULTI BOARD ARCHITECTURE



Prior Art

Figure 3

# IC WITH uP INTERFACE AND LOCAL BUS INTERFACE



Prior Art

20200303 14:55:33

# IC WITH LOCAL BUS INTERFACE

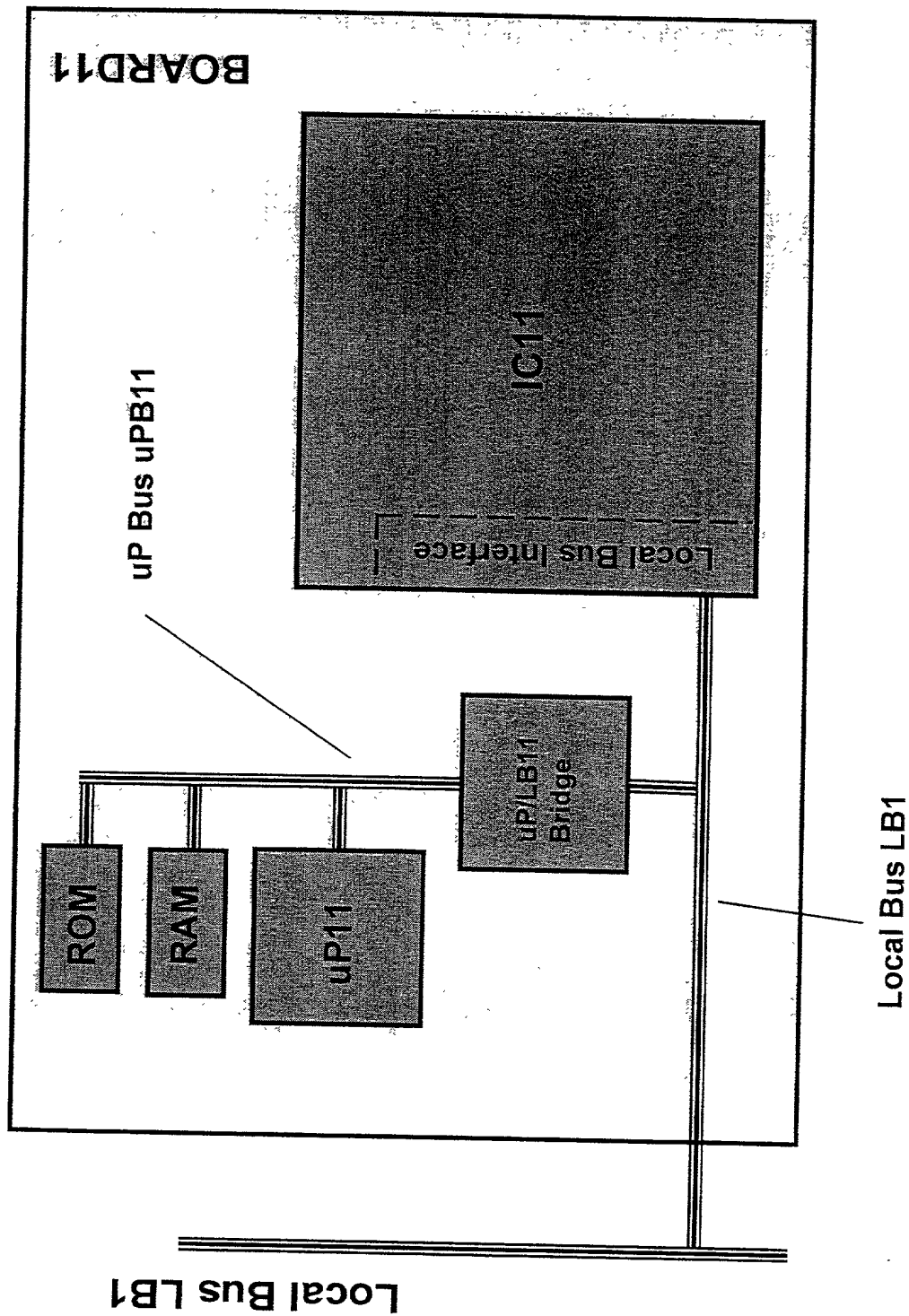
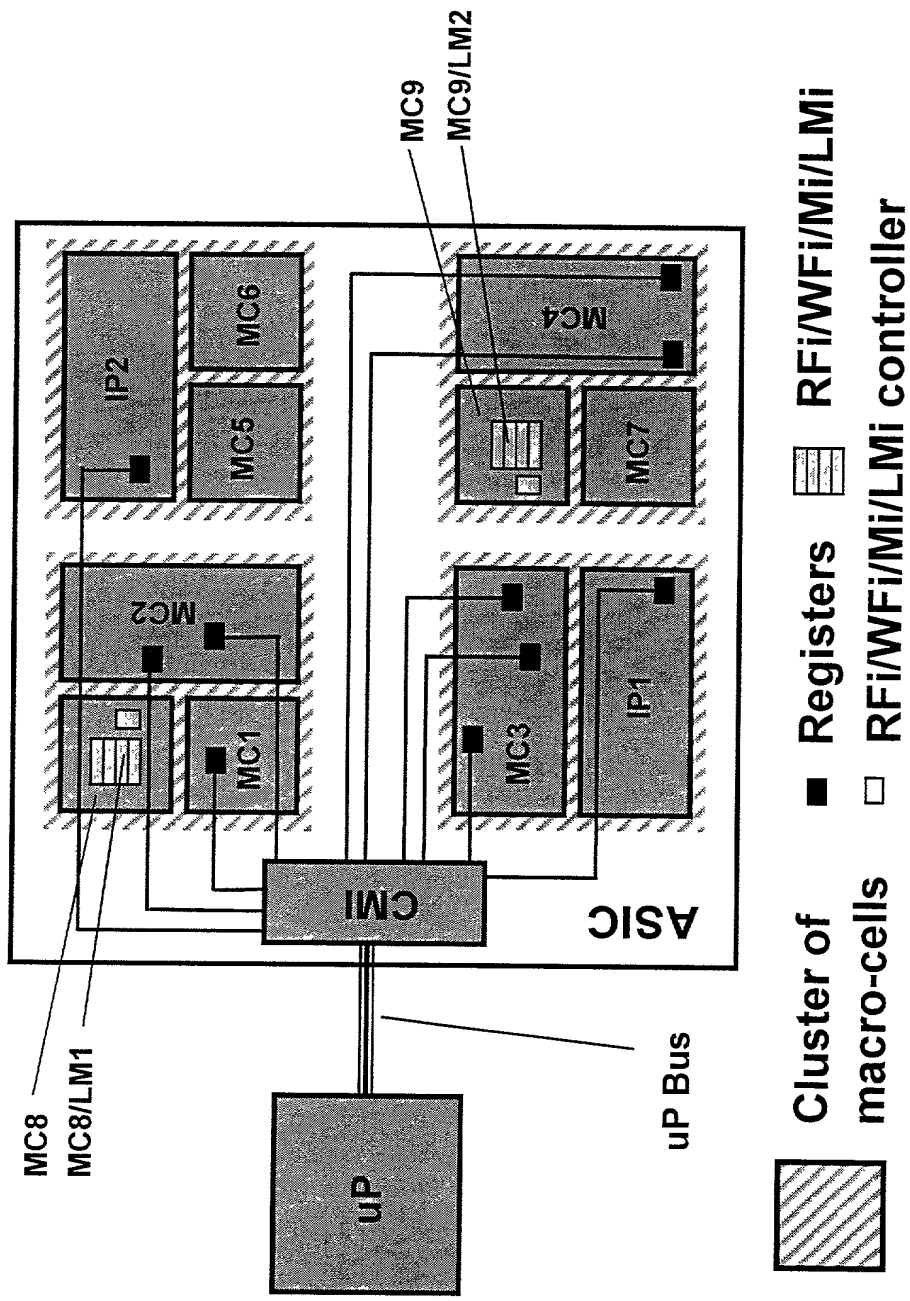


Figure 4

Prior Art

Figure 5

# ASIC implementation of CMI with C MPI macro-cells interface



Prior Art

Figure 6

# ASIC implementation of CMI with CBBI macro-cells interface

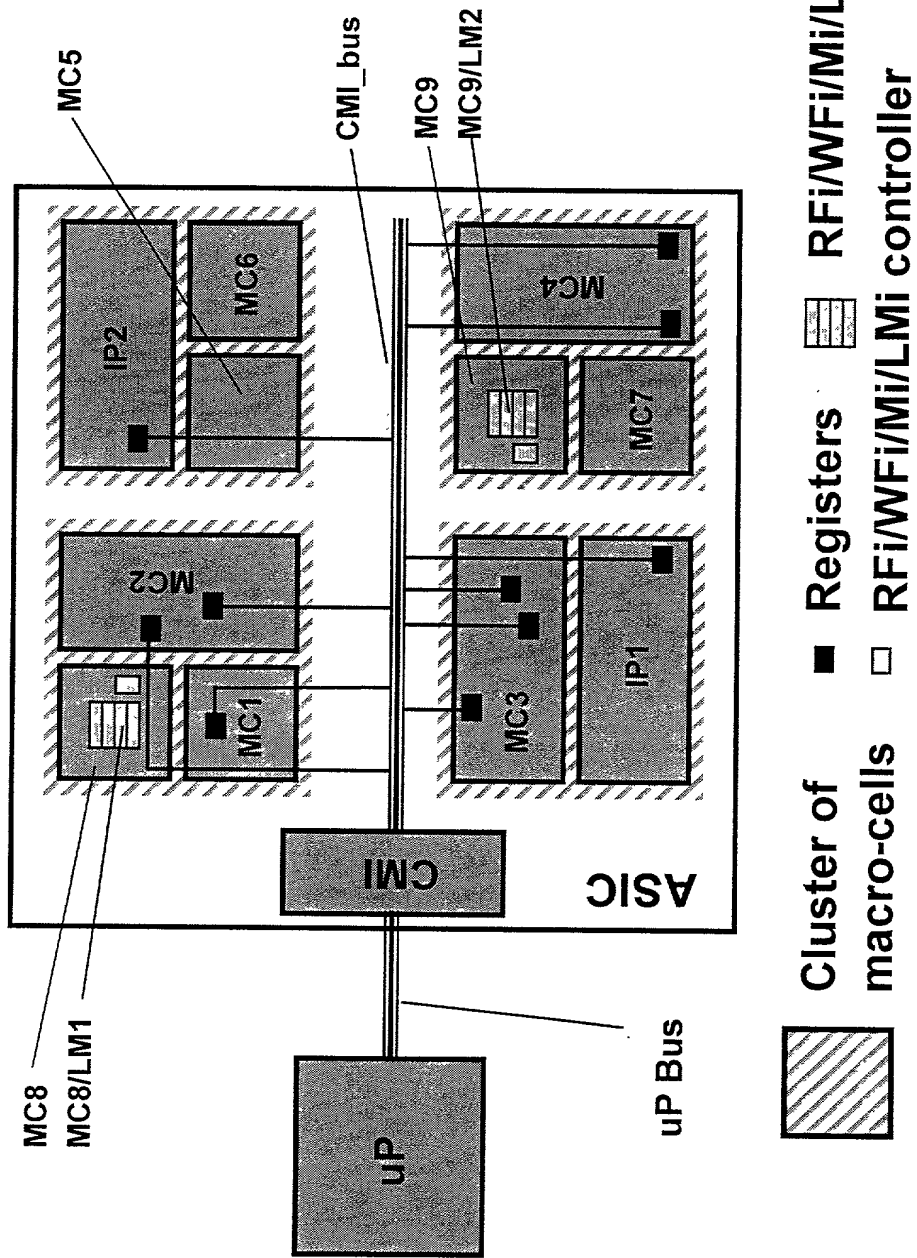
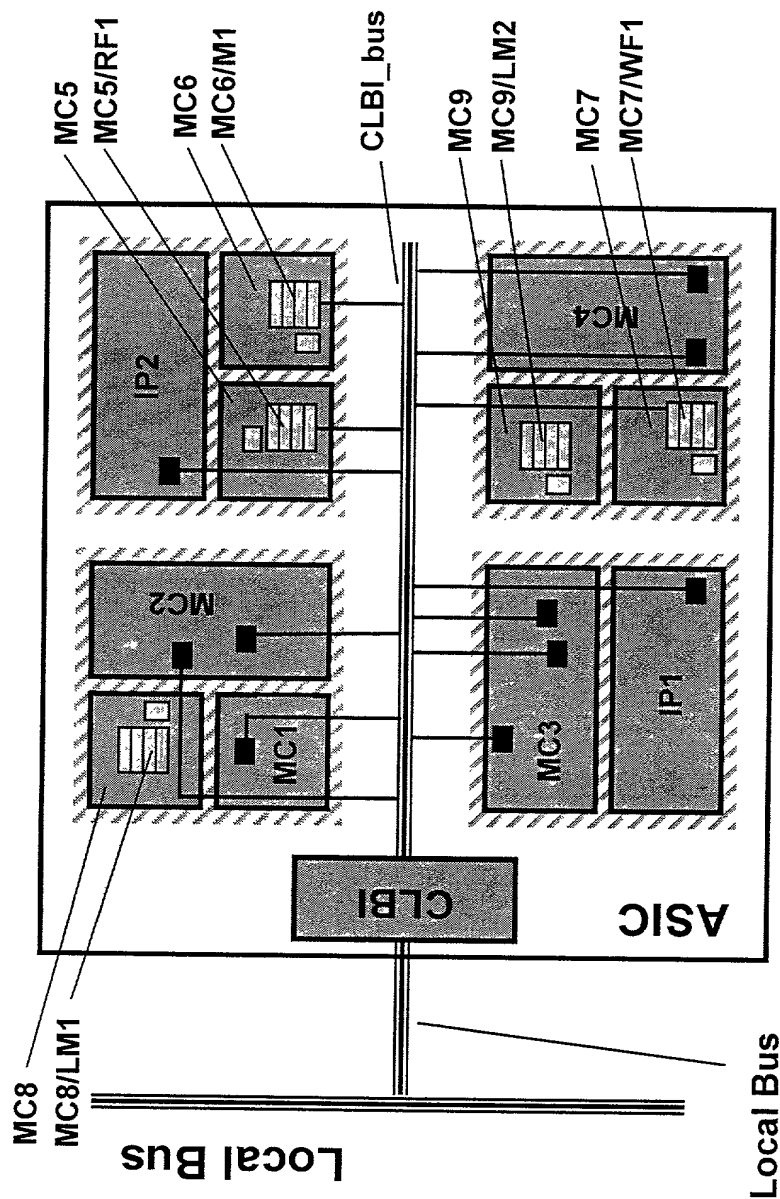


Figure 7

# ASIC implementation of CLBI with CBBi macro-cells interface



- Cluster of macro-cells
- Registers
- RFi/WFi/Mi/LMi
- RFi/WFi/Mi/LMi controller

Figure 8

# ASIC implementation of CLBI with CMPI macro-cells interface

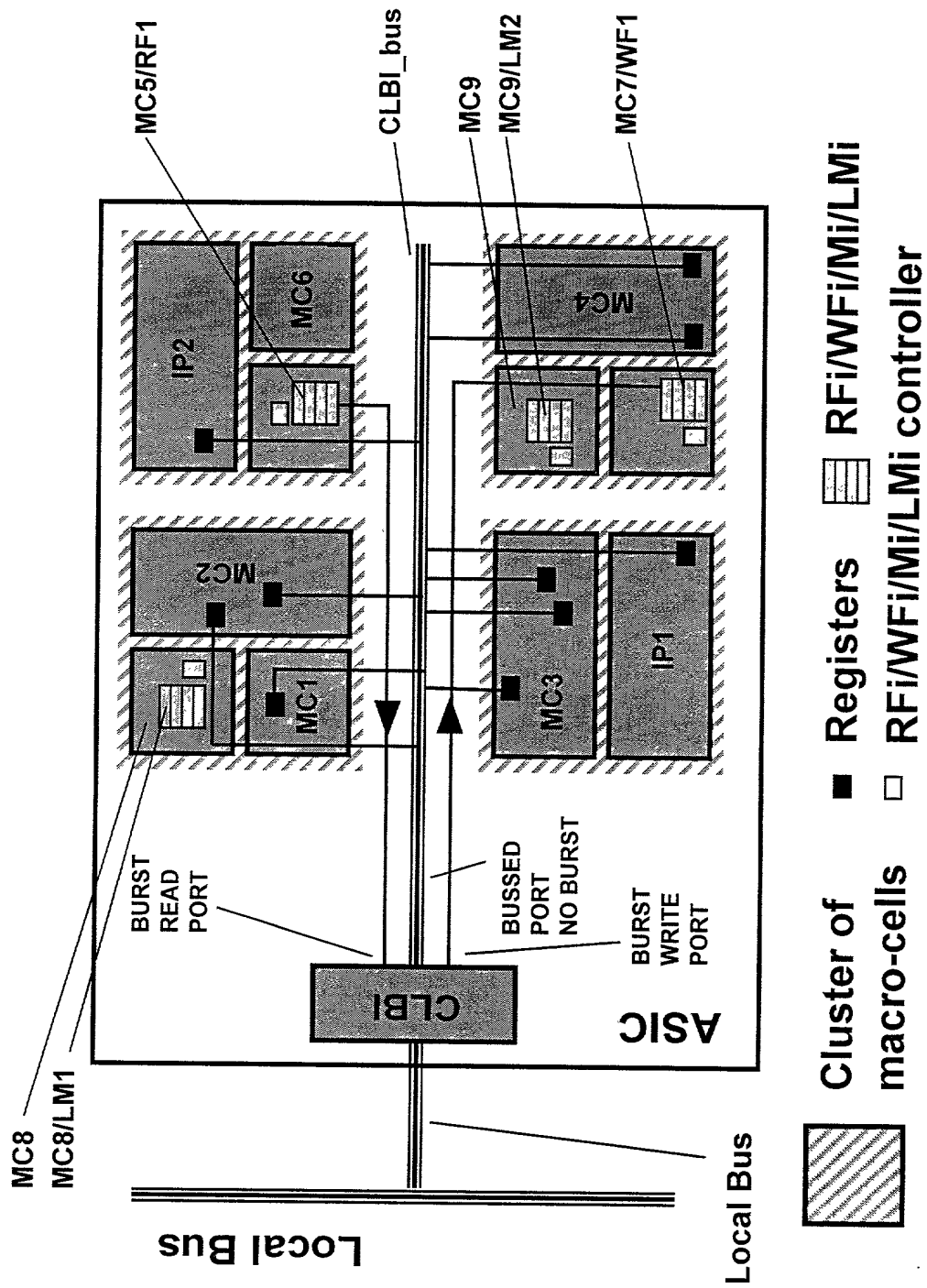




Figure 9

# Board hosting ASIC implementation of AAL5 interfaced via DMI

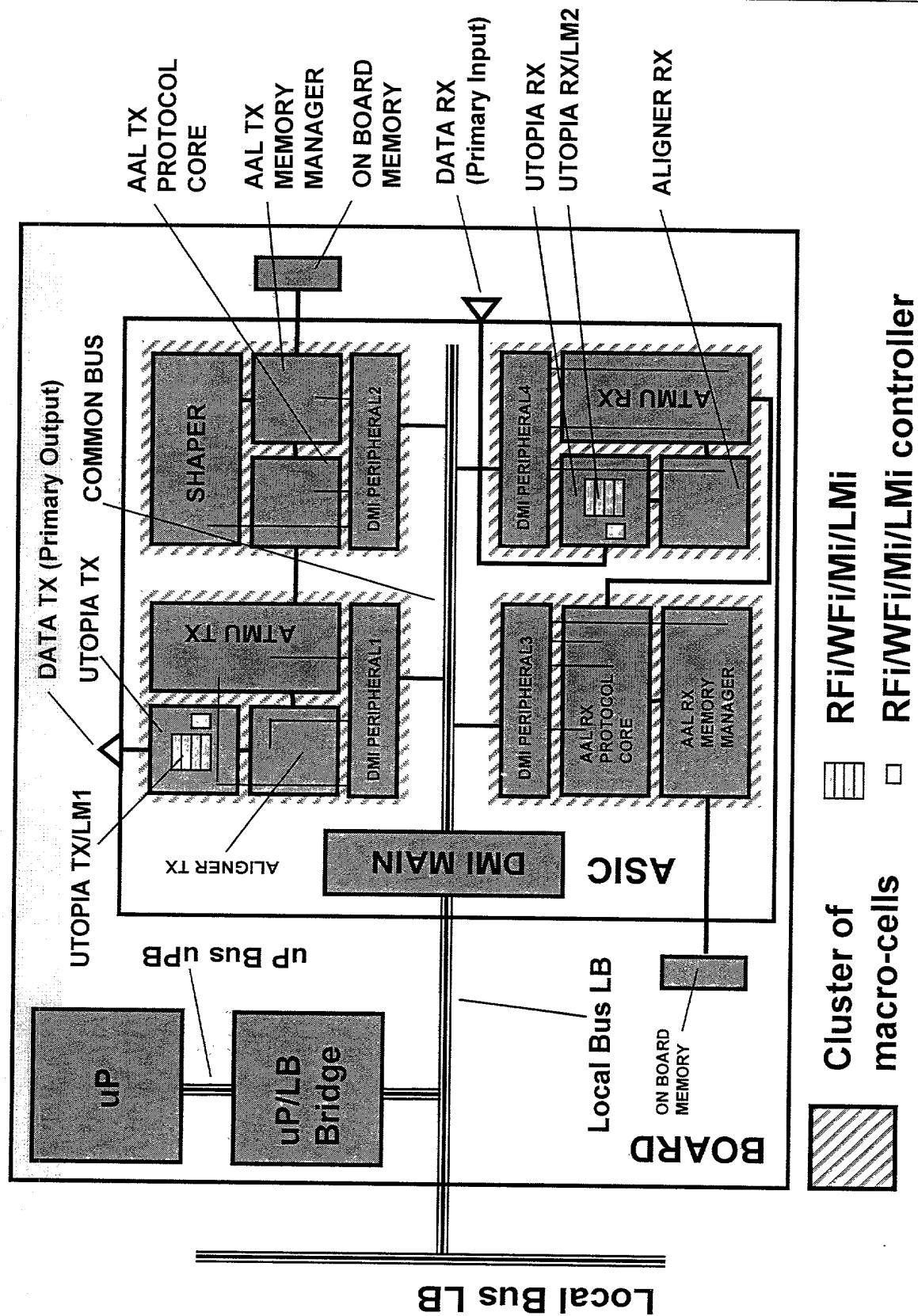
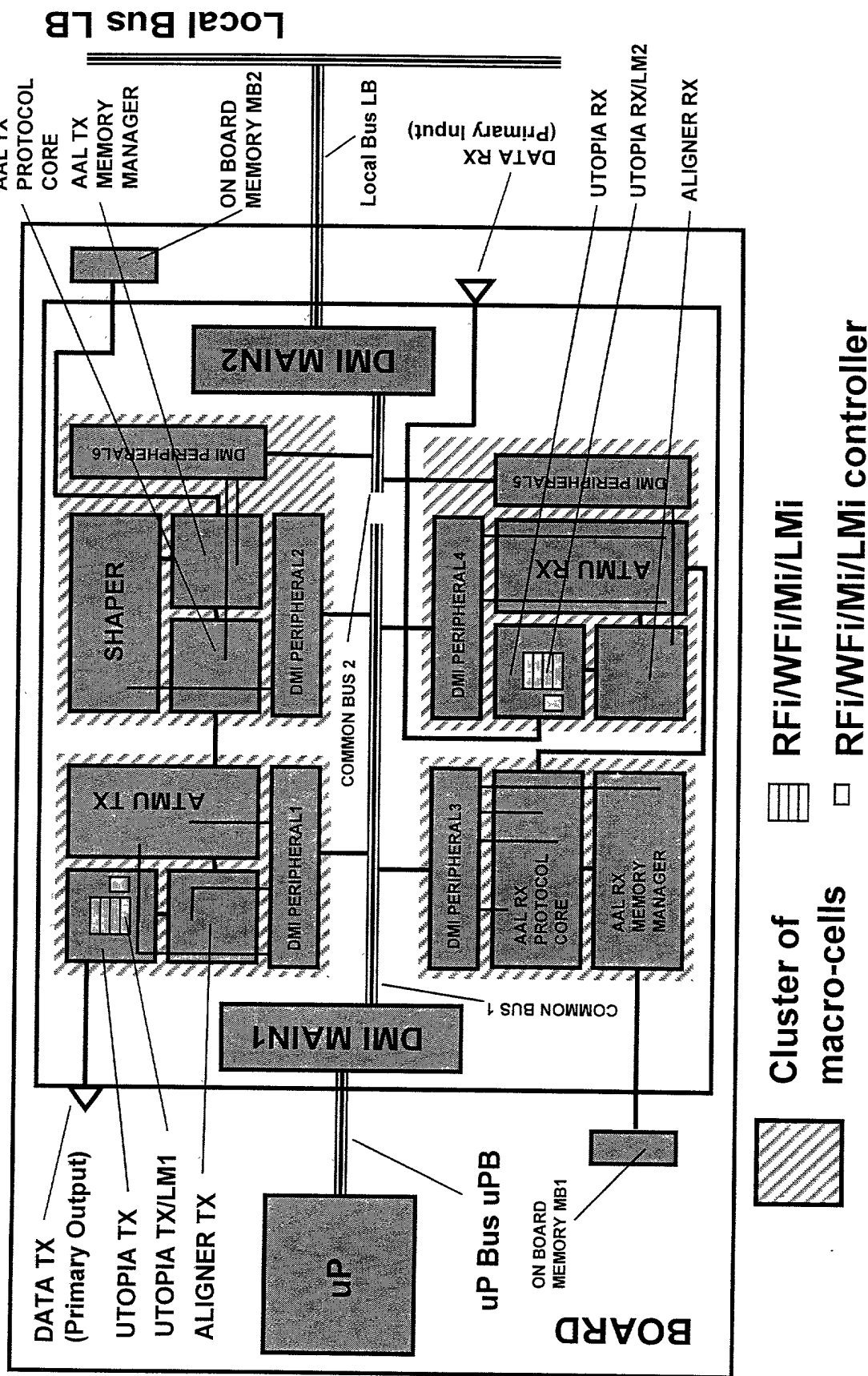


Figure 10

# Board hosting FPGA bread-boarding implementation of a DMI for microprocessor interface and a DMI for local bus interface



## Board hosting FPGA bread-boarding implementation of DMI

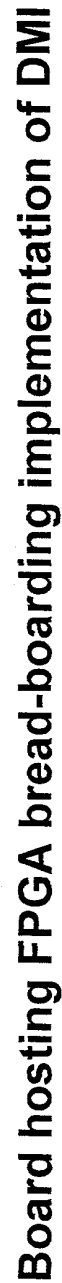
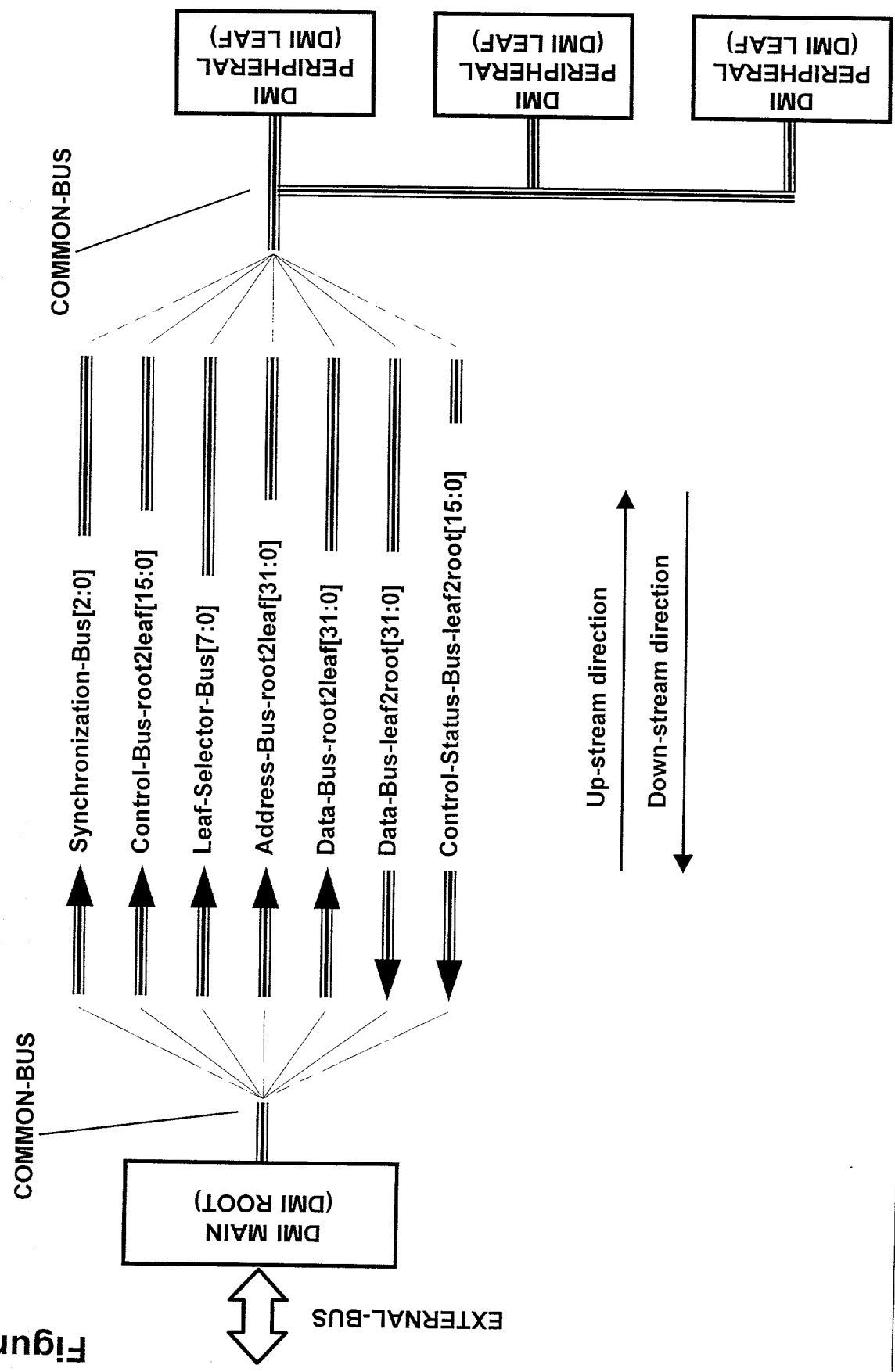


Figure 12

# COMMON BUS exploded in sub-buses



*[Faint, illegible handwritten notes or bleed-through from the reverse side of the page.]*

### Figure 13

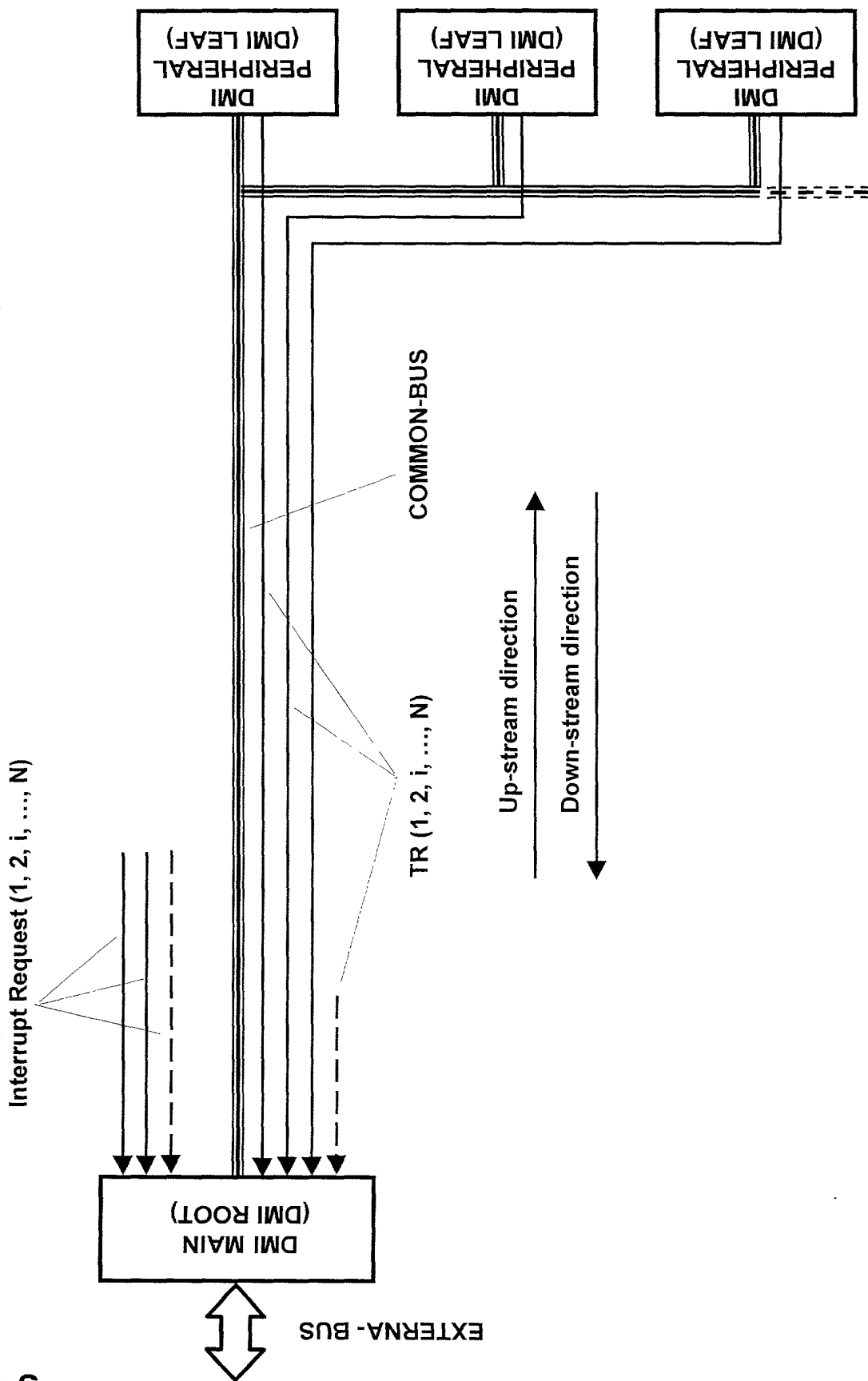


Figure 14

# DMI MAIN INTERNAL ARCHITECTURE

Plug-In module

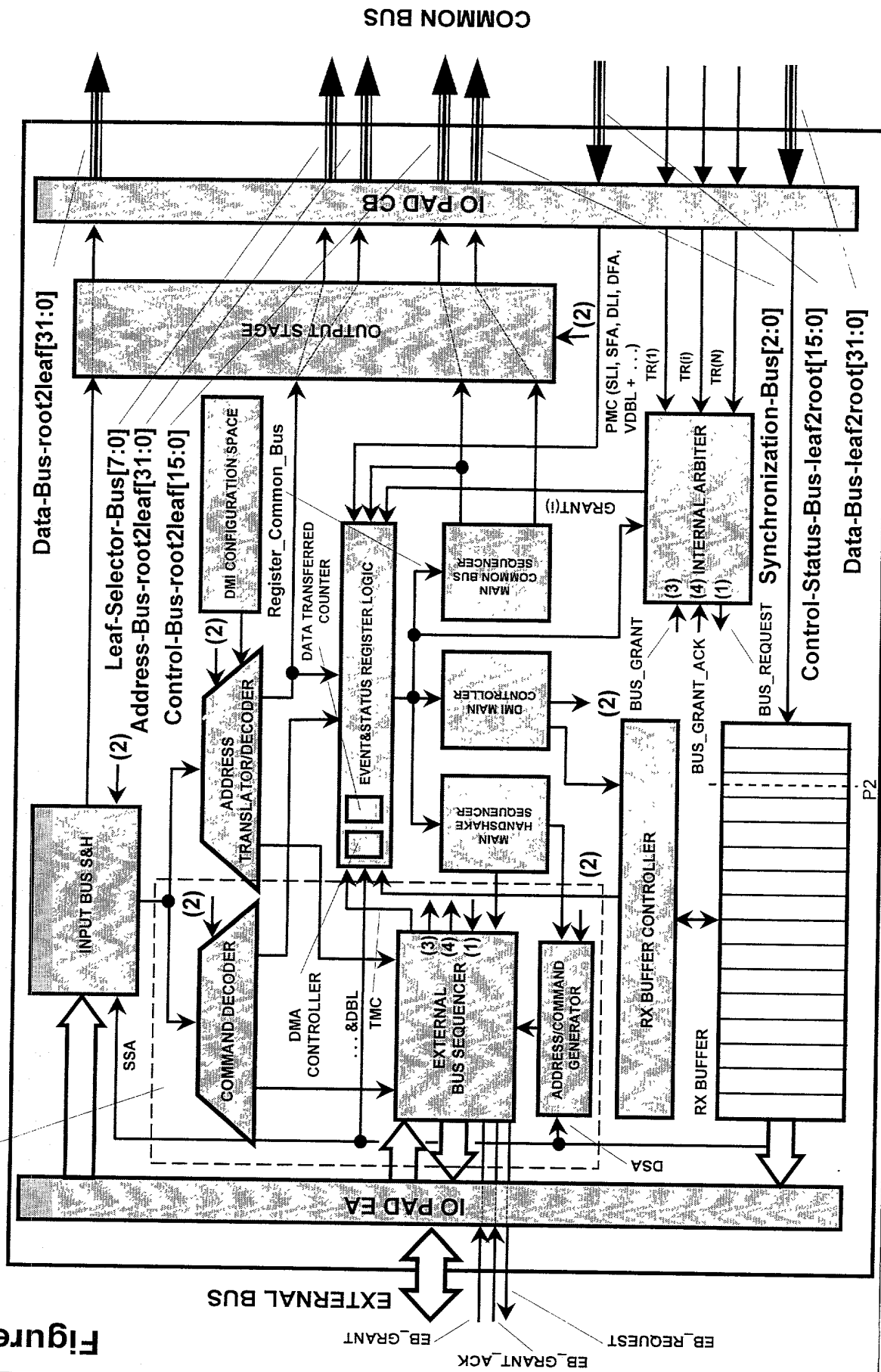


Figure 15 DMI compliant macro-cell basic architecture

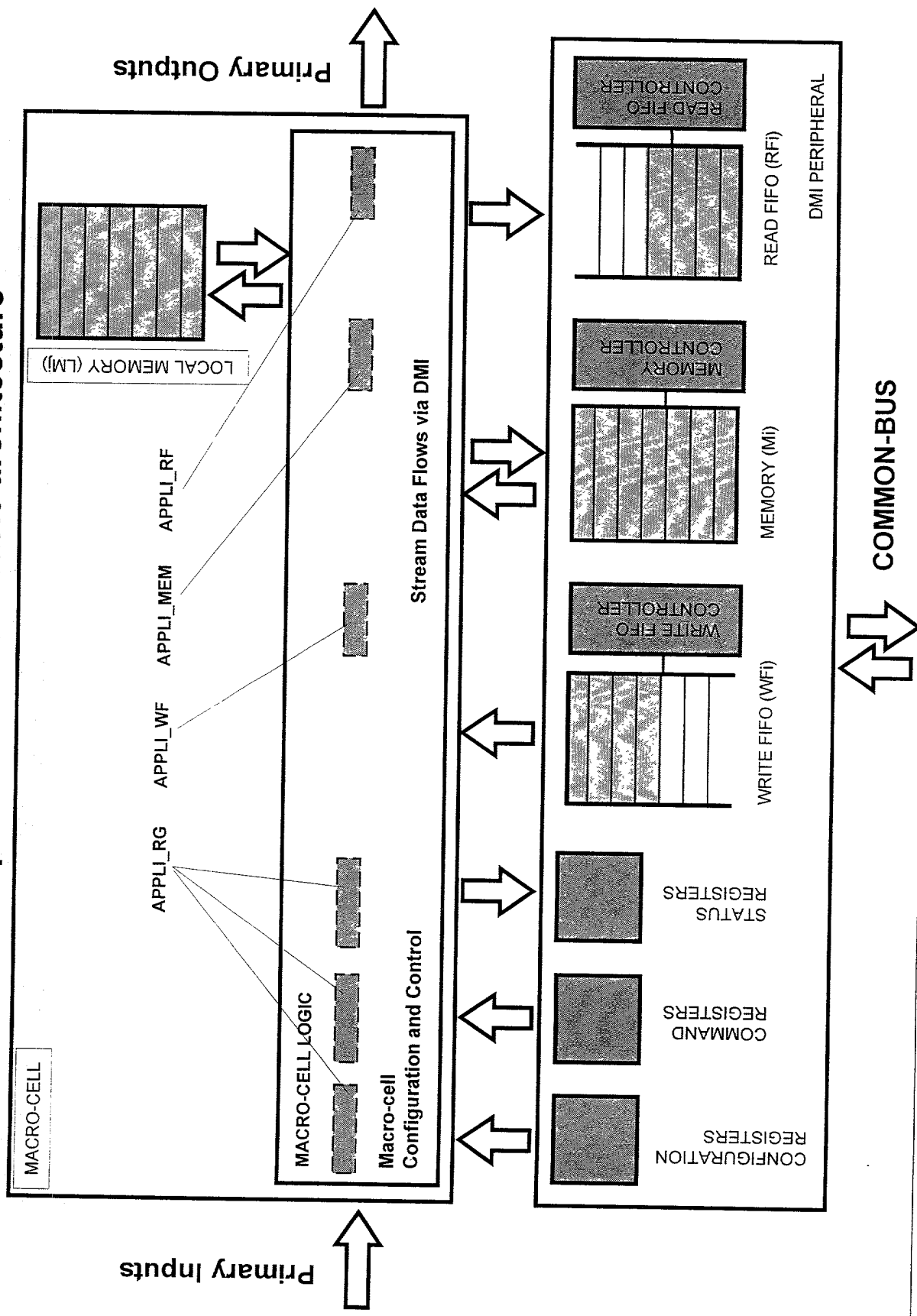


Figure 16

# DMI PERIPHERAL Shadowed Layers

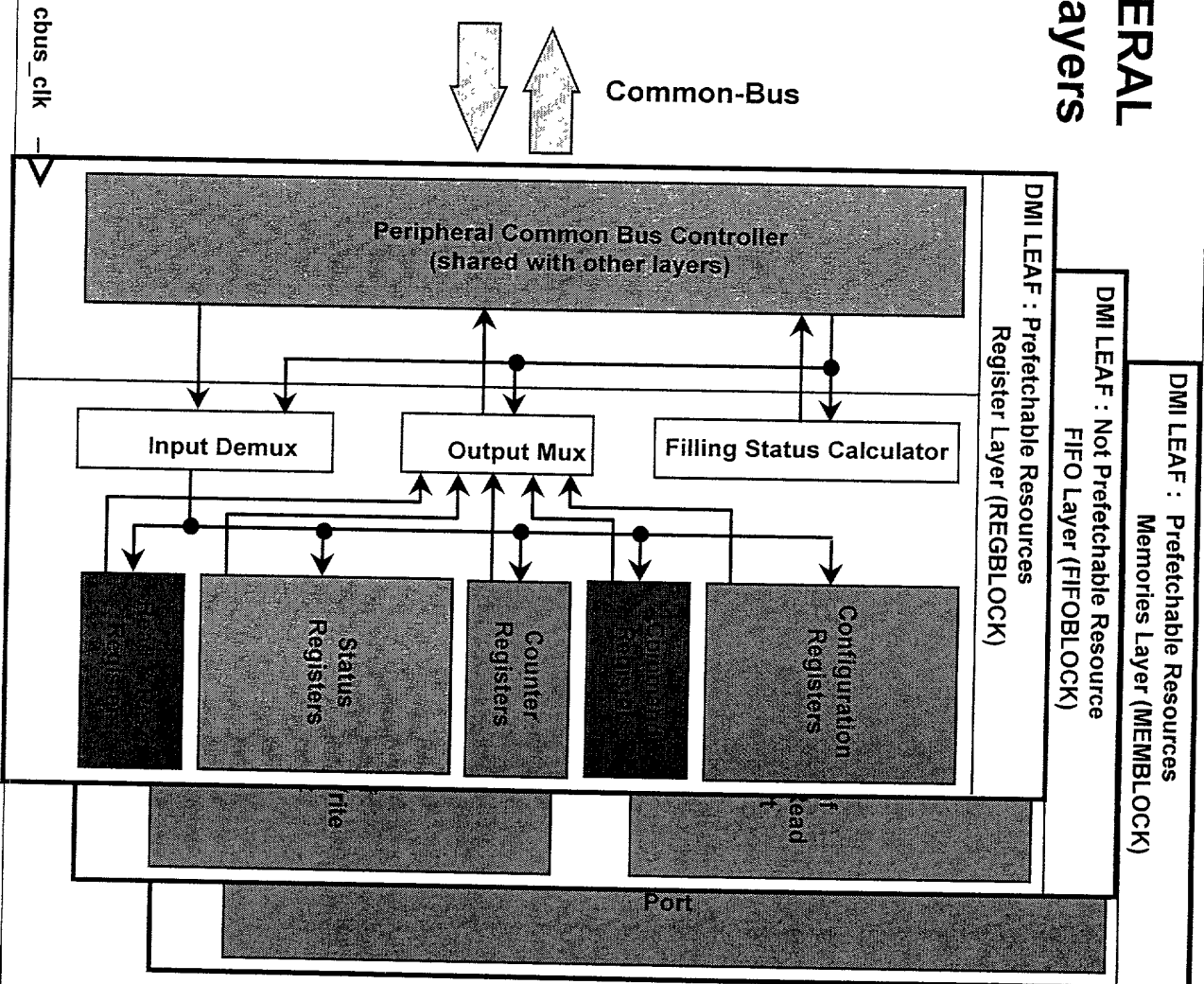


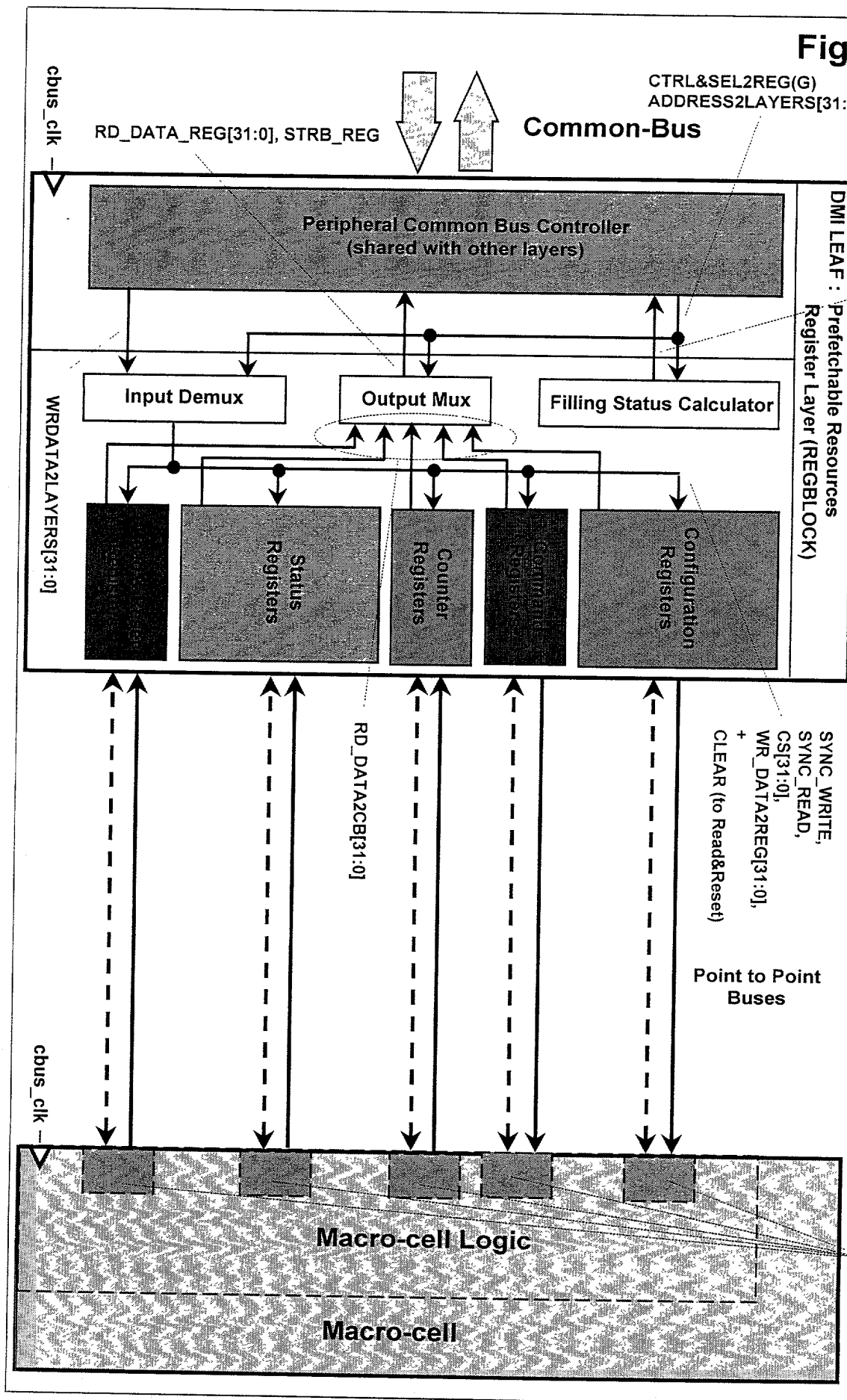




Figure 18

# DMILEAF : Prefetchable Resources - Registers Layer (REGBLOCK)

FS\_REG[4:0]



## DMI LEAF : Prefetchable Resources - Registers Layer (REGBLOCK)

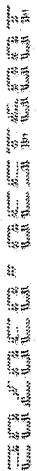
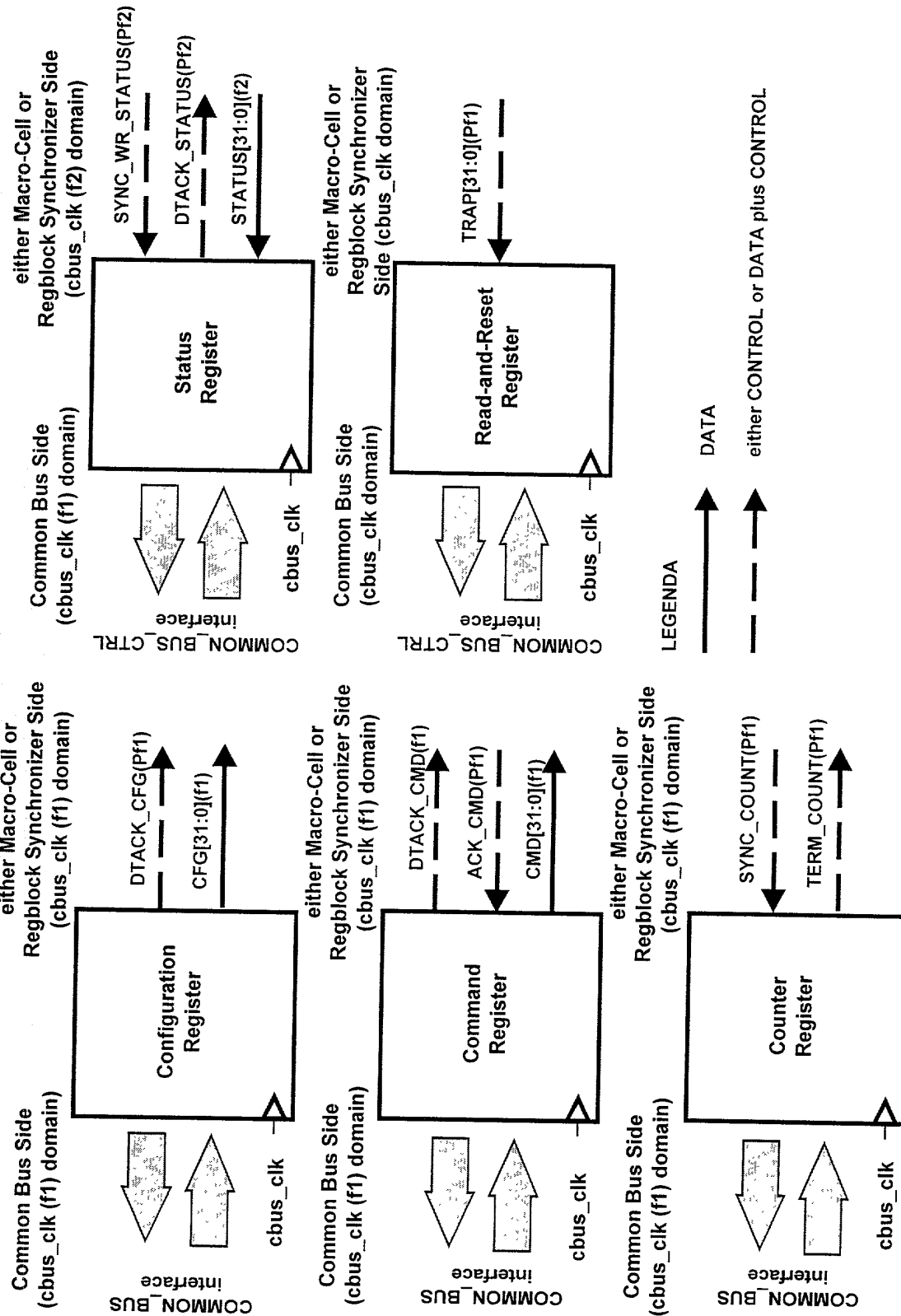


Figure 20

# REGBLOCK Register Types



NOTE referred to Counter Register:  
DATA\_FROM\_CB[31:0] is THRESHOLD[31:0]  
DATA2CB[31:0] is COUNTER[31:0]

Figure 21

# REGBLOCK SYNCHRONIZER Register Synchronizer Types

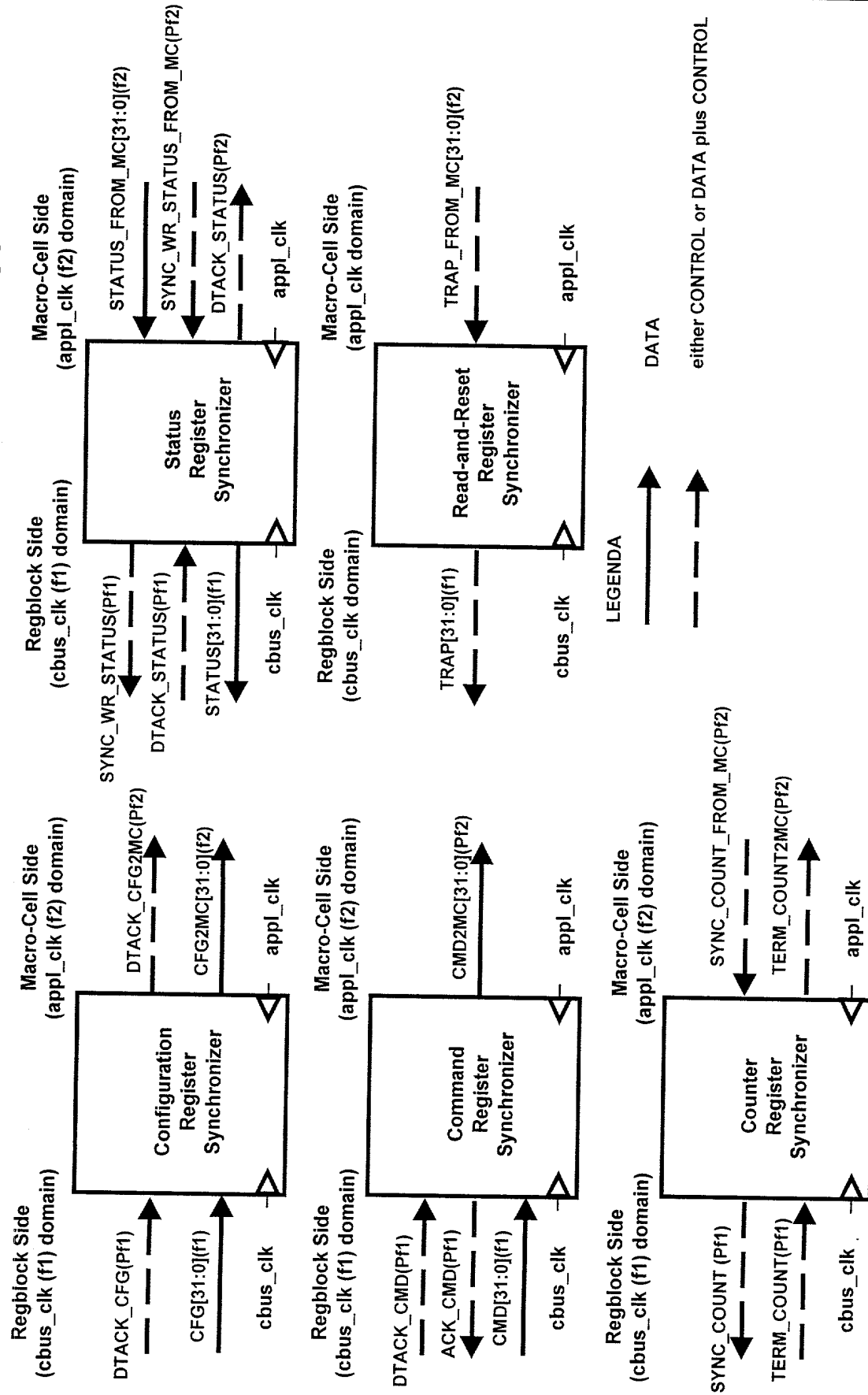


Figure 22

# DMI LEAF : Prefetchable Resources - Memories Layer (MEMBLOCK)

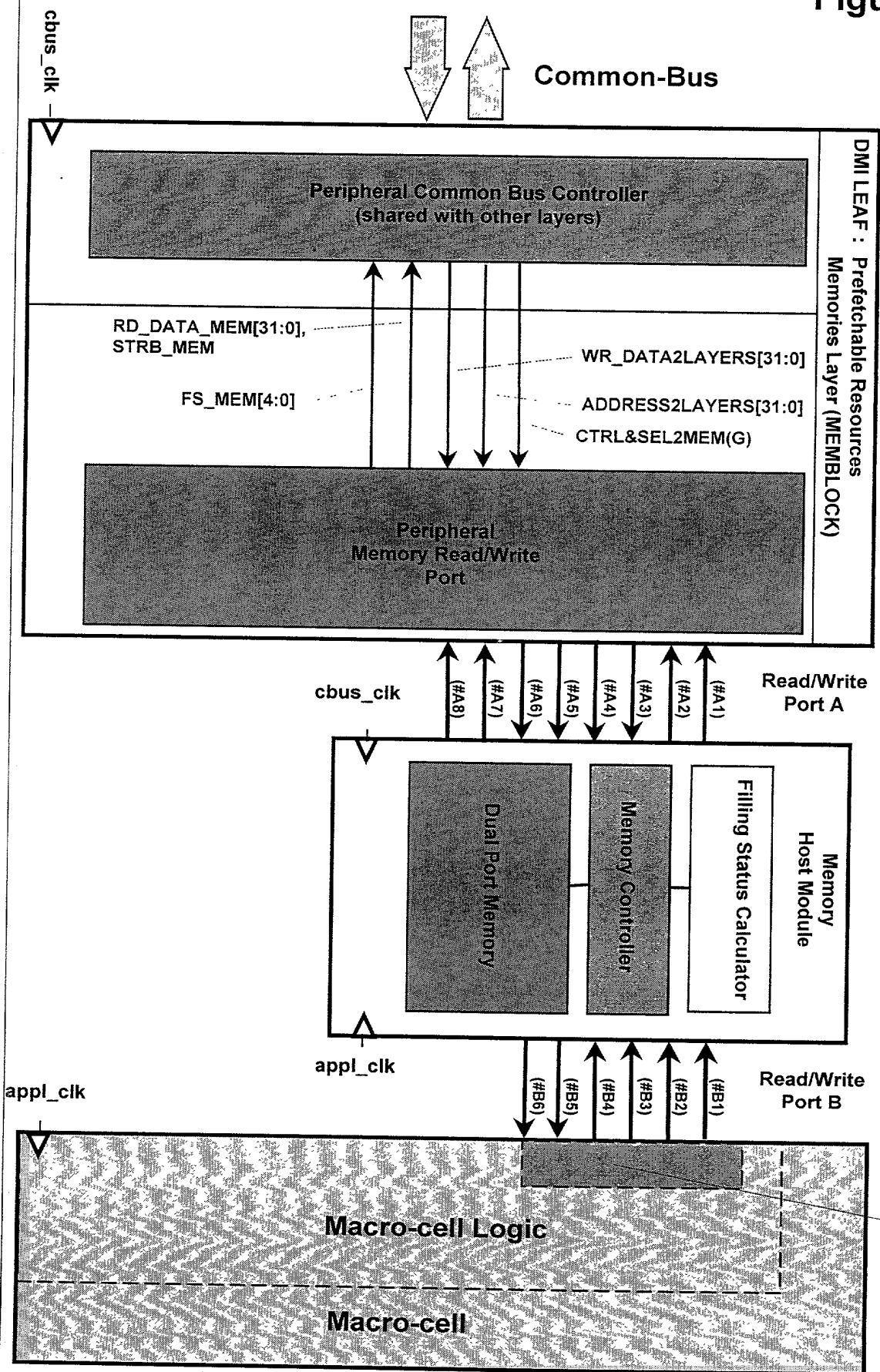


Figure 23

# DMI LEAF : Not Prefetchable Resources FIFO Layer (FIFOBLOCK)

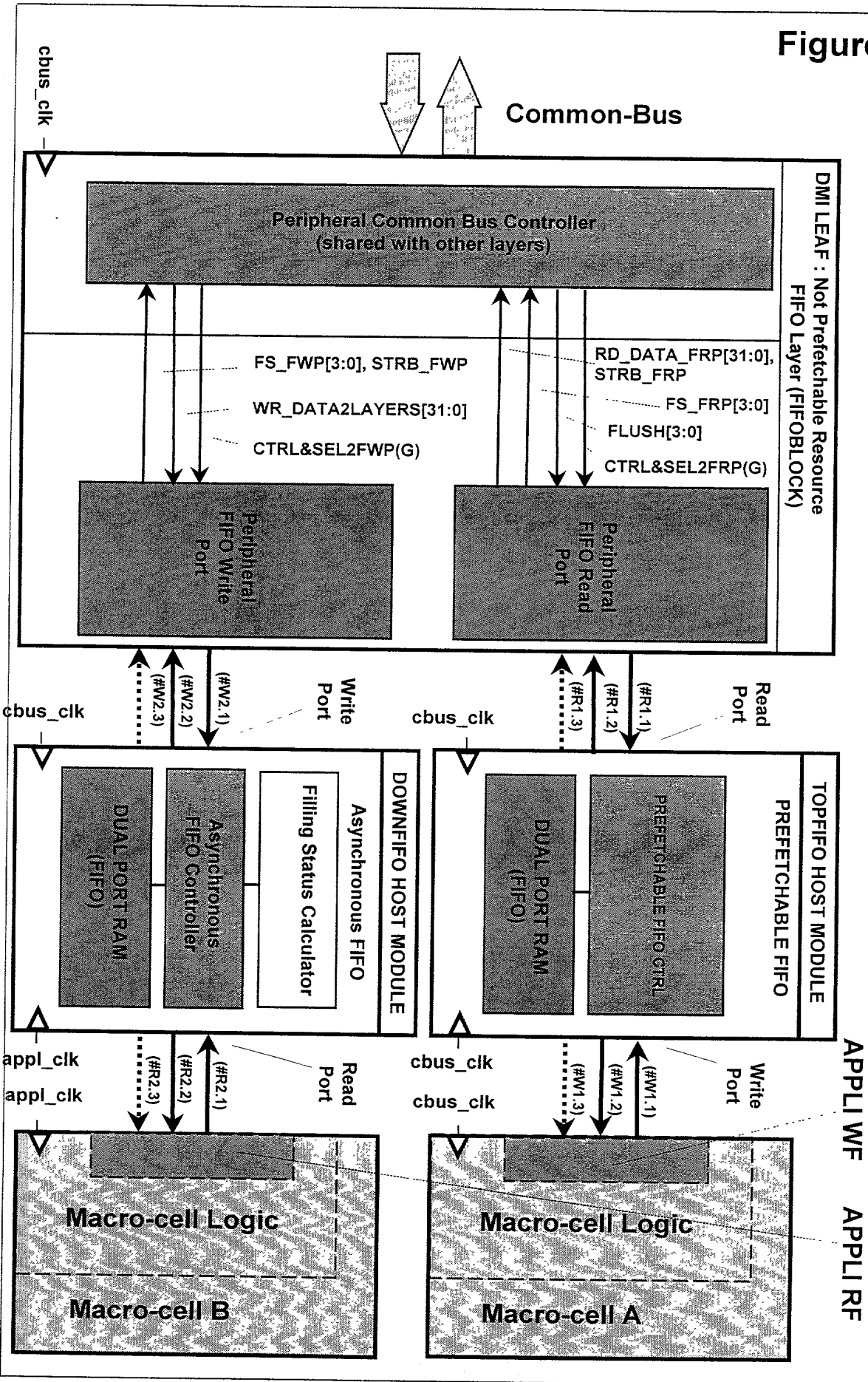
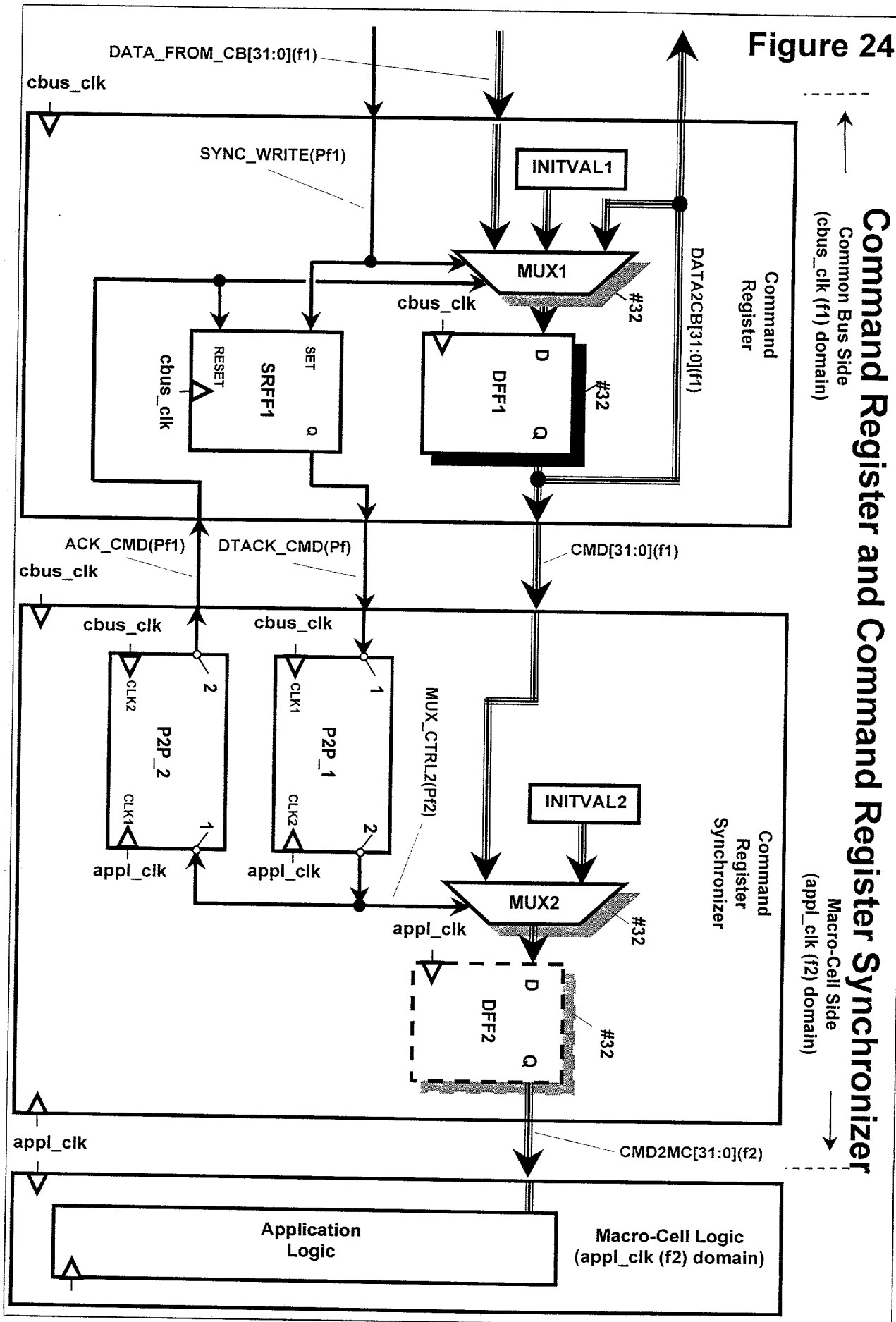




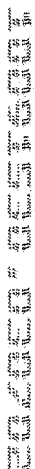
Figure 24

# Command Register and Command Register Synchronizer





## Status Register and Status Register Synchronizer



# Pulse to Pulse Synchronization Unit

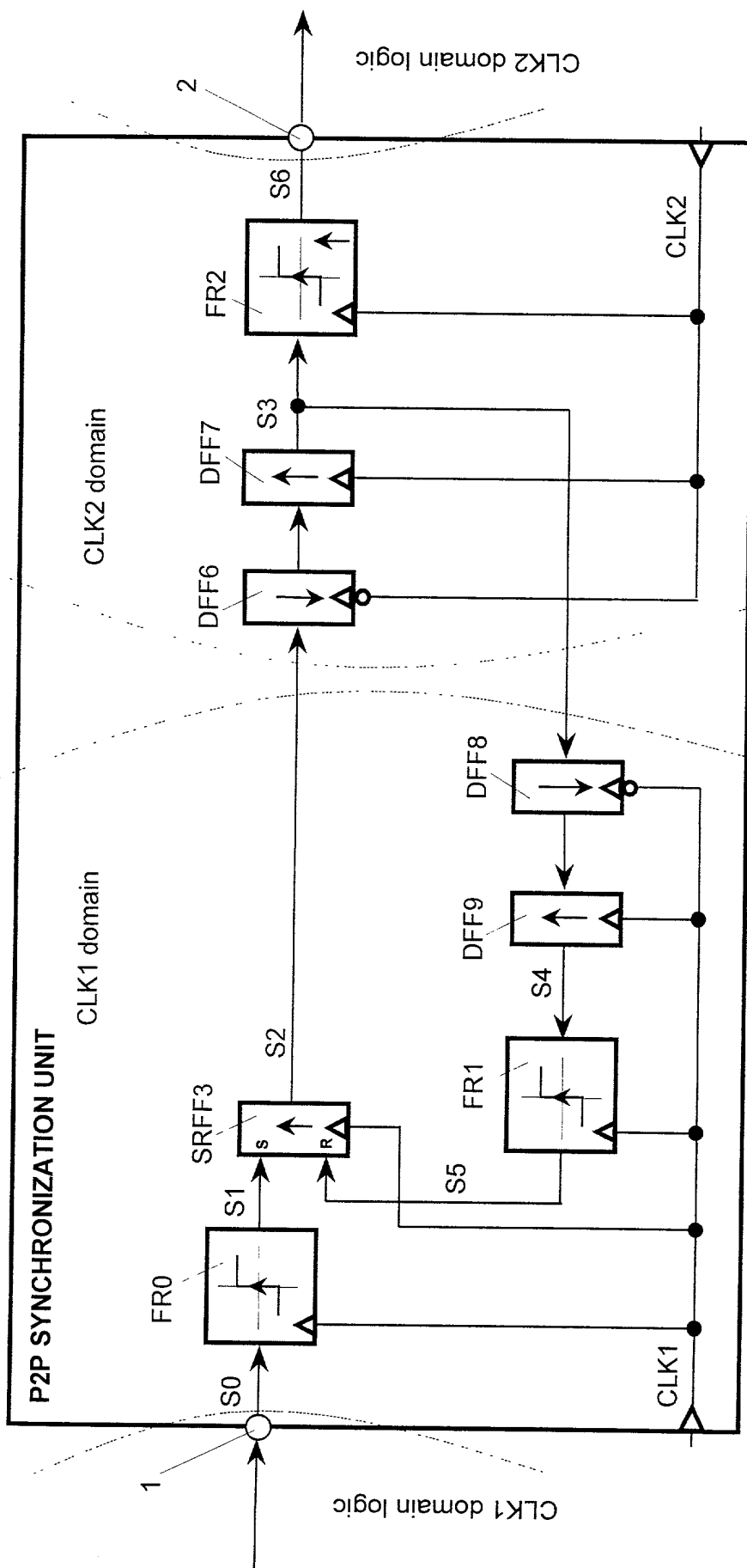


Figure 26

Figure 27

## Timing Diagram of Pulse to Pulse Synchronization Unit

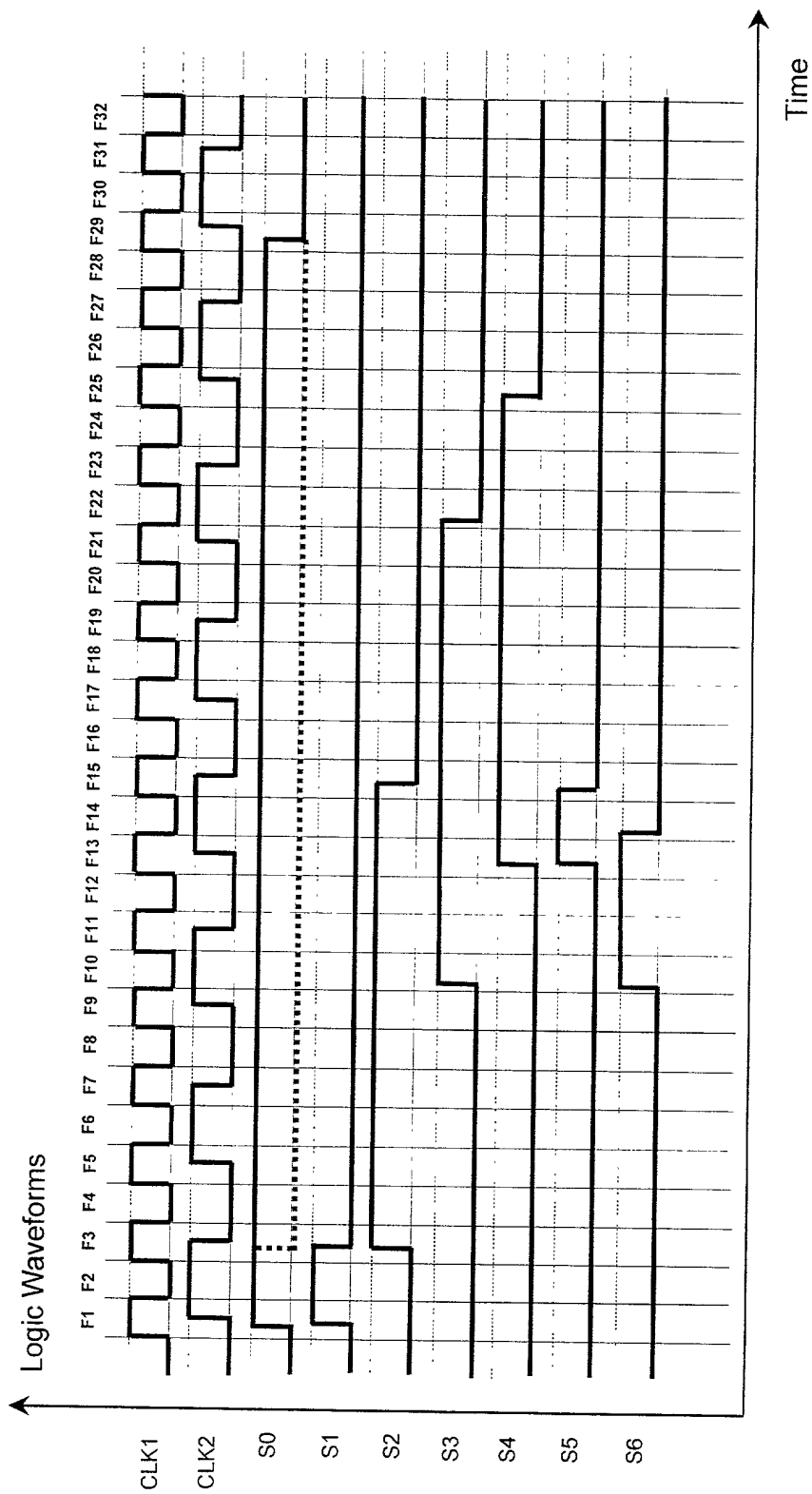


Figure 28

# Advantages of Distributed Synchronization

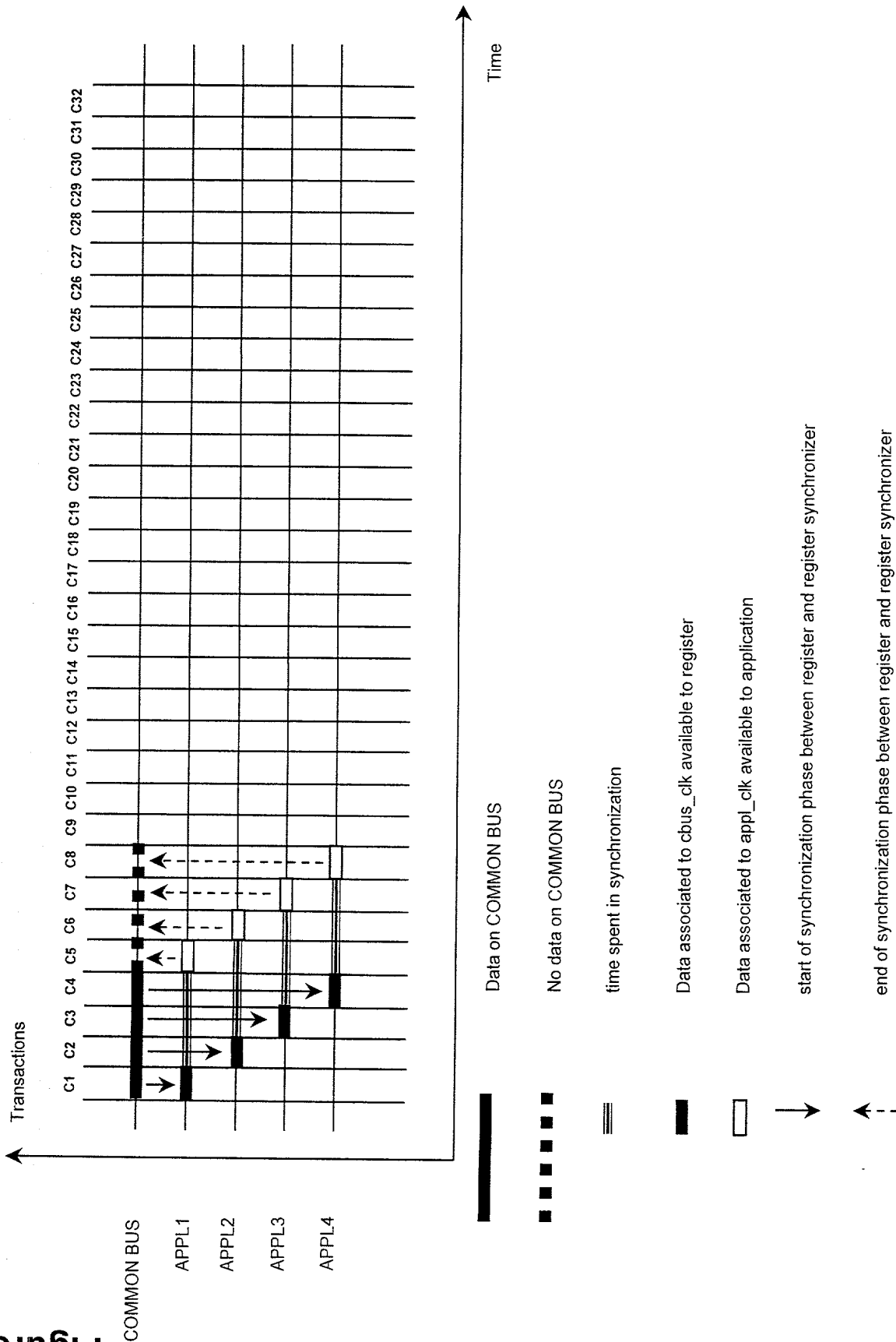
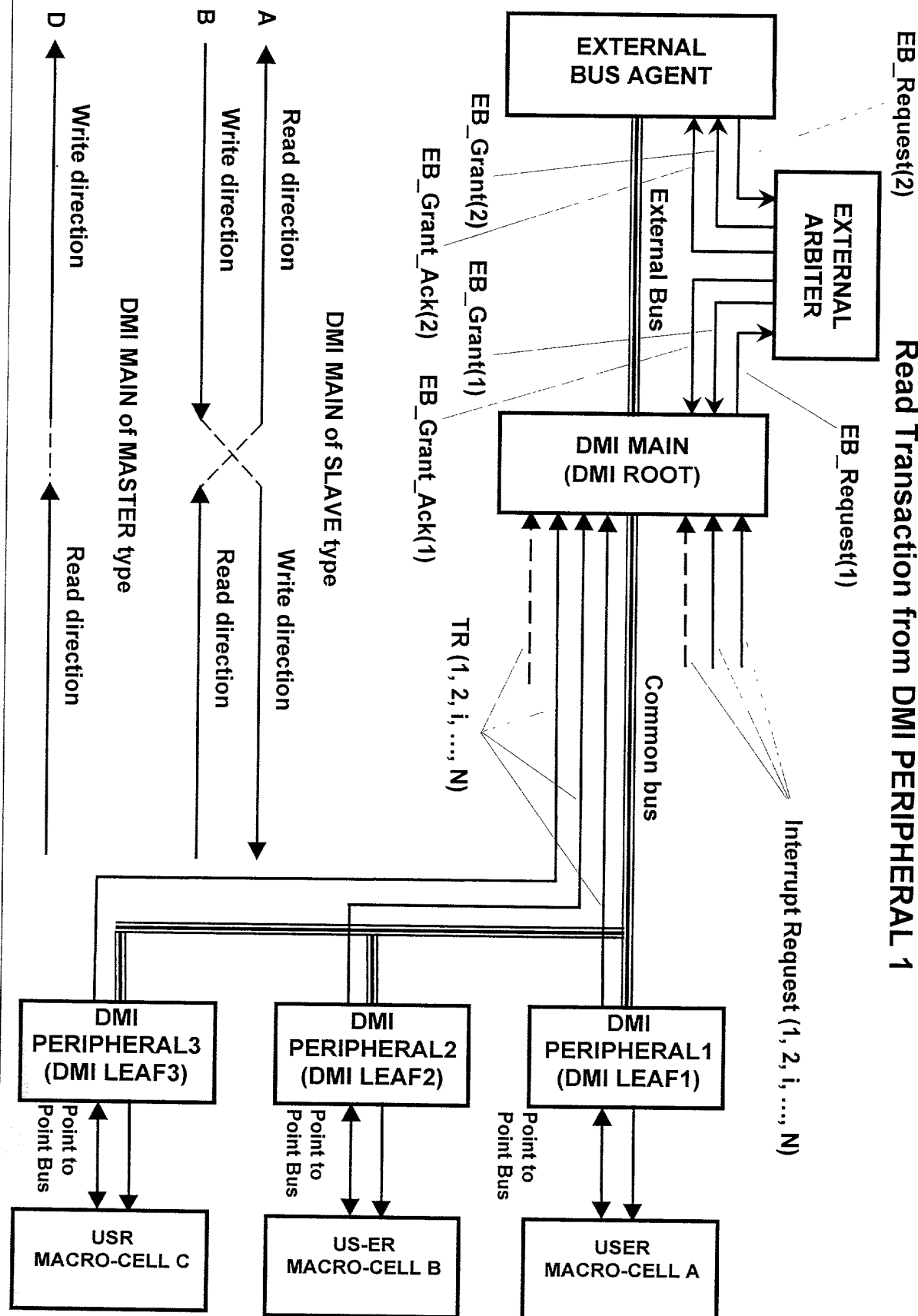
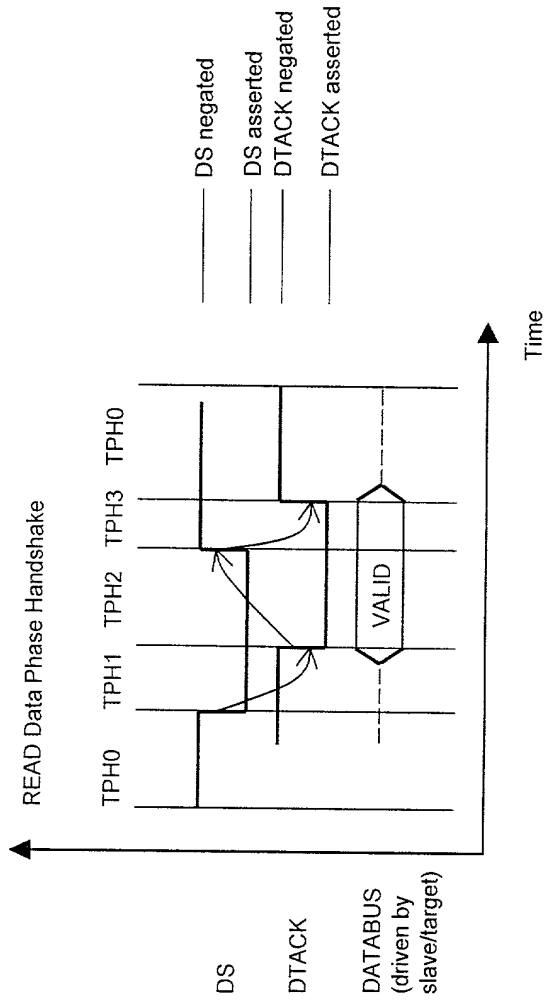


Figure 29

EXTERNAL BUS AGENT DMI acting as Master  
Read Transaction from DMI PERIPHERAL 1



Asynchronous two phase handshake protocol: read



Asynchronous two phase handshake protocol: write

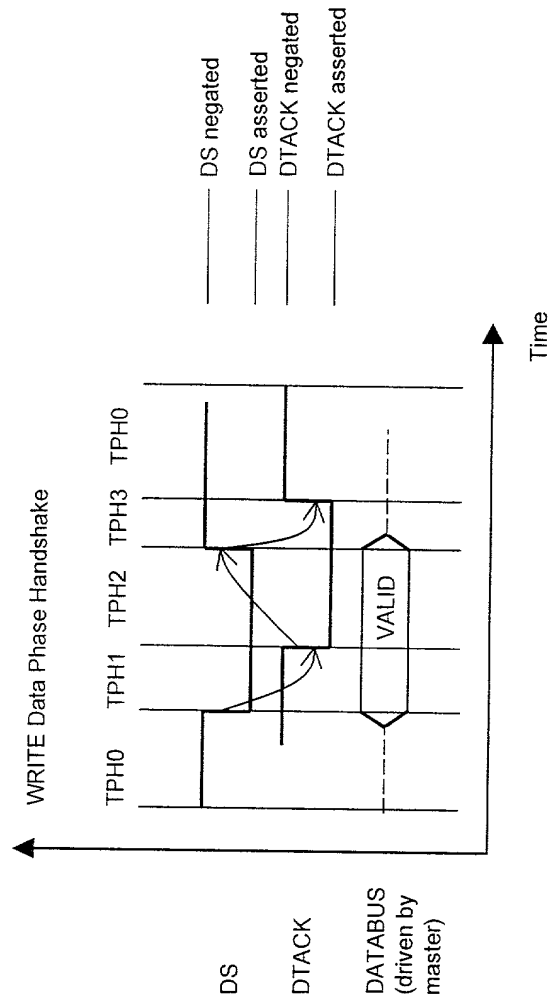


Figure 32

Prior Art

EBA-DMI ROOT interface  
MASTER: EBA  
SLAVE: DMI ROOT

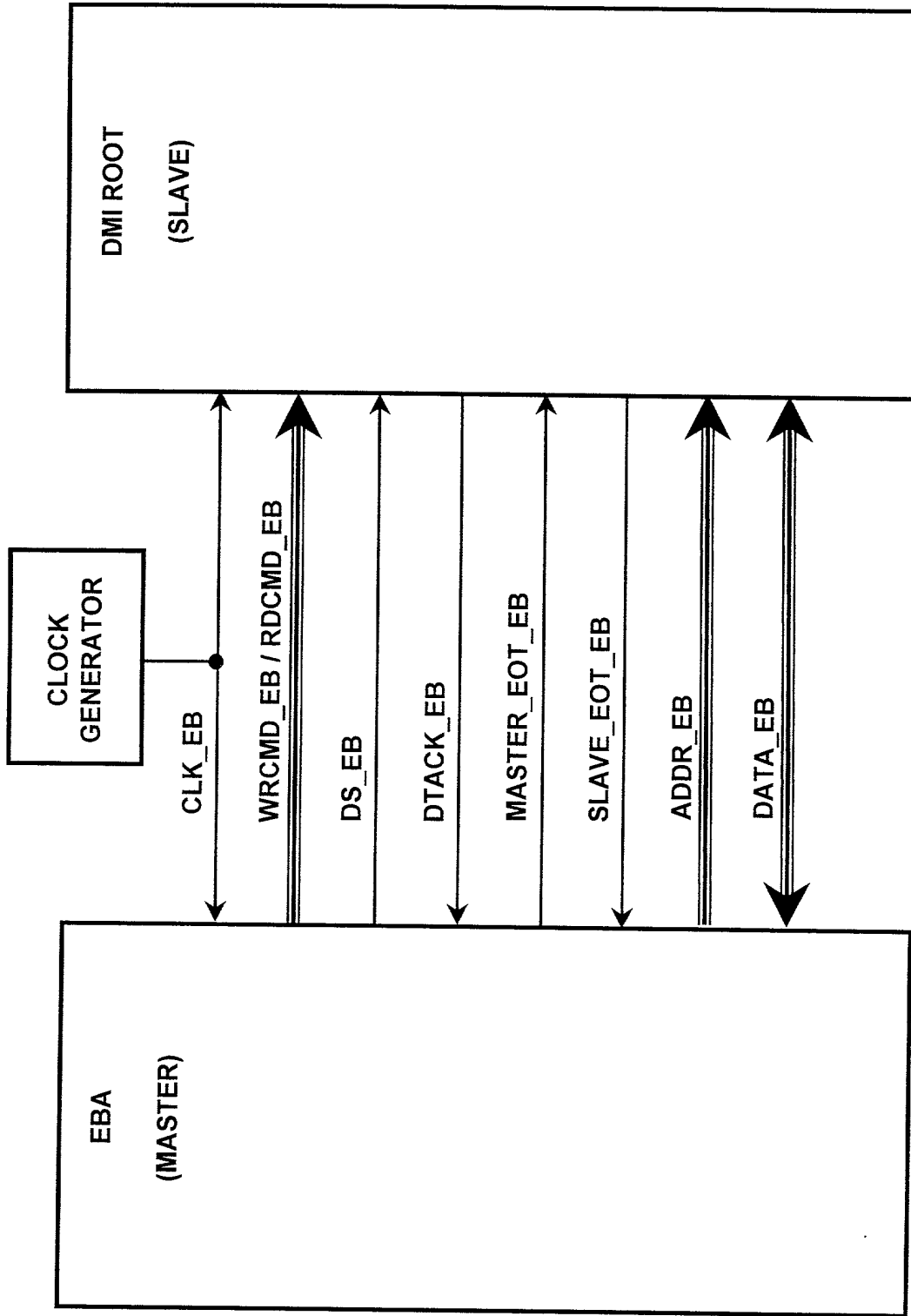
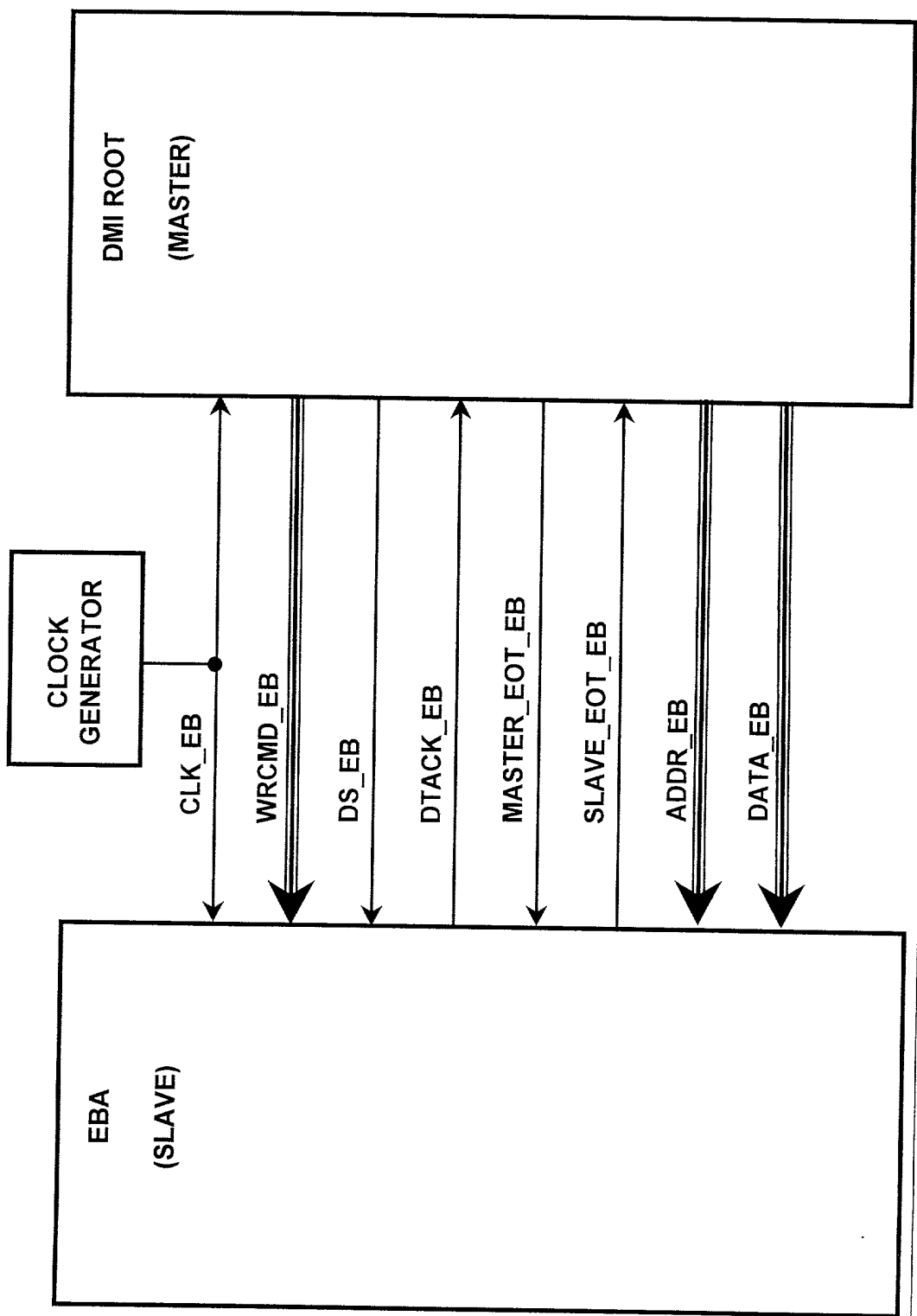




Figure 33

Prior Art

EBA-DMI ROOT interface  
MASTER: DMI ROOT  
SLAVE: EBA



## DMI PERIPHERAL support for Transaction Requesters

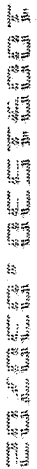


Figure 35

# DMI Slave Mode Overall Algorithm Representation Read Transaction from DMI PERIPHERAL + Read Transaction from EXTERNAL BUS AGENT

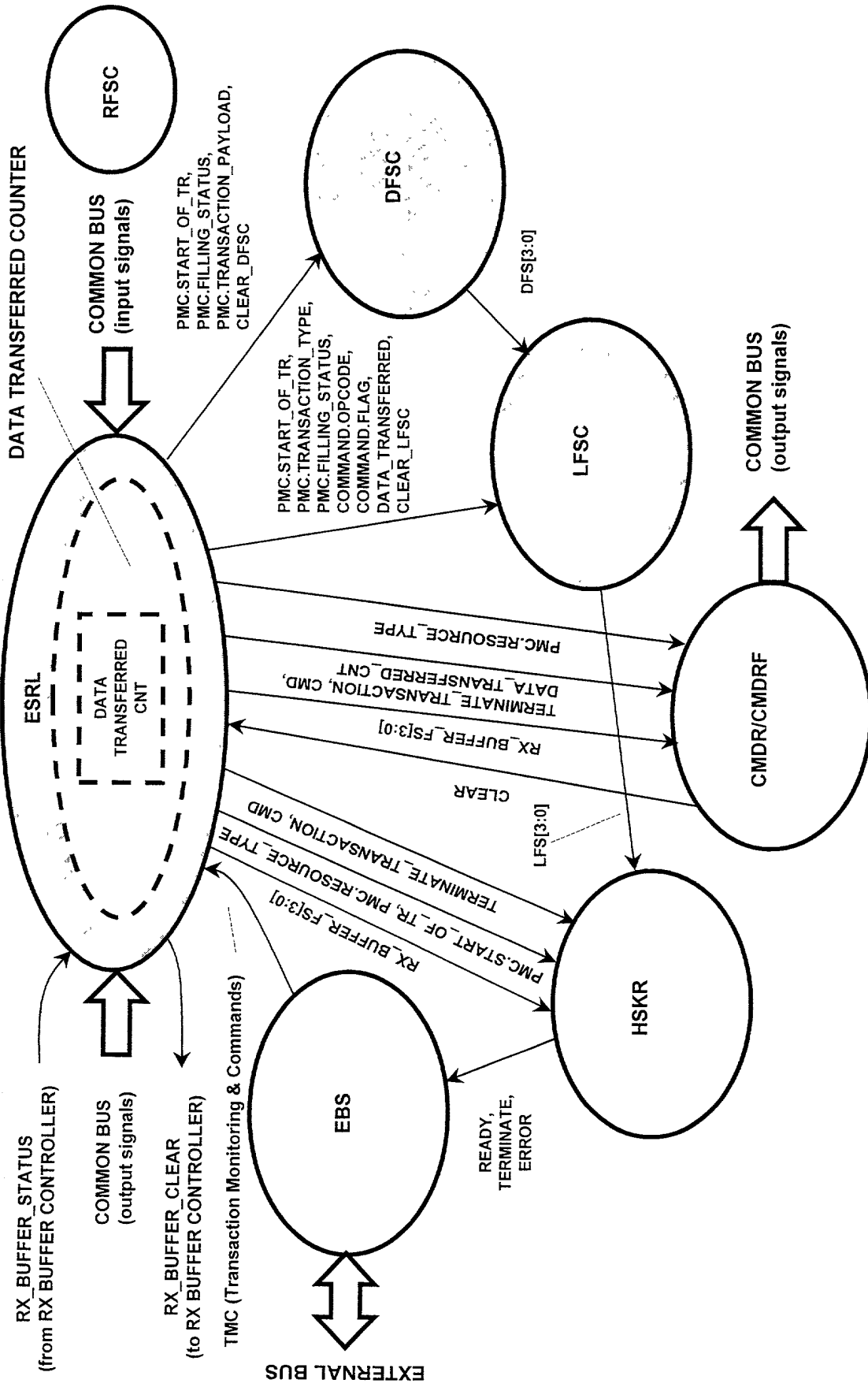


Figure 36

# Message Sequence Chart

EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
 Burst READ Transaction from DMI PERIPHERAL1/ Prefetchable resource  
 EXTERNAL BUS AGENT (master) Termination

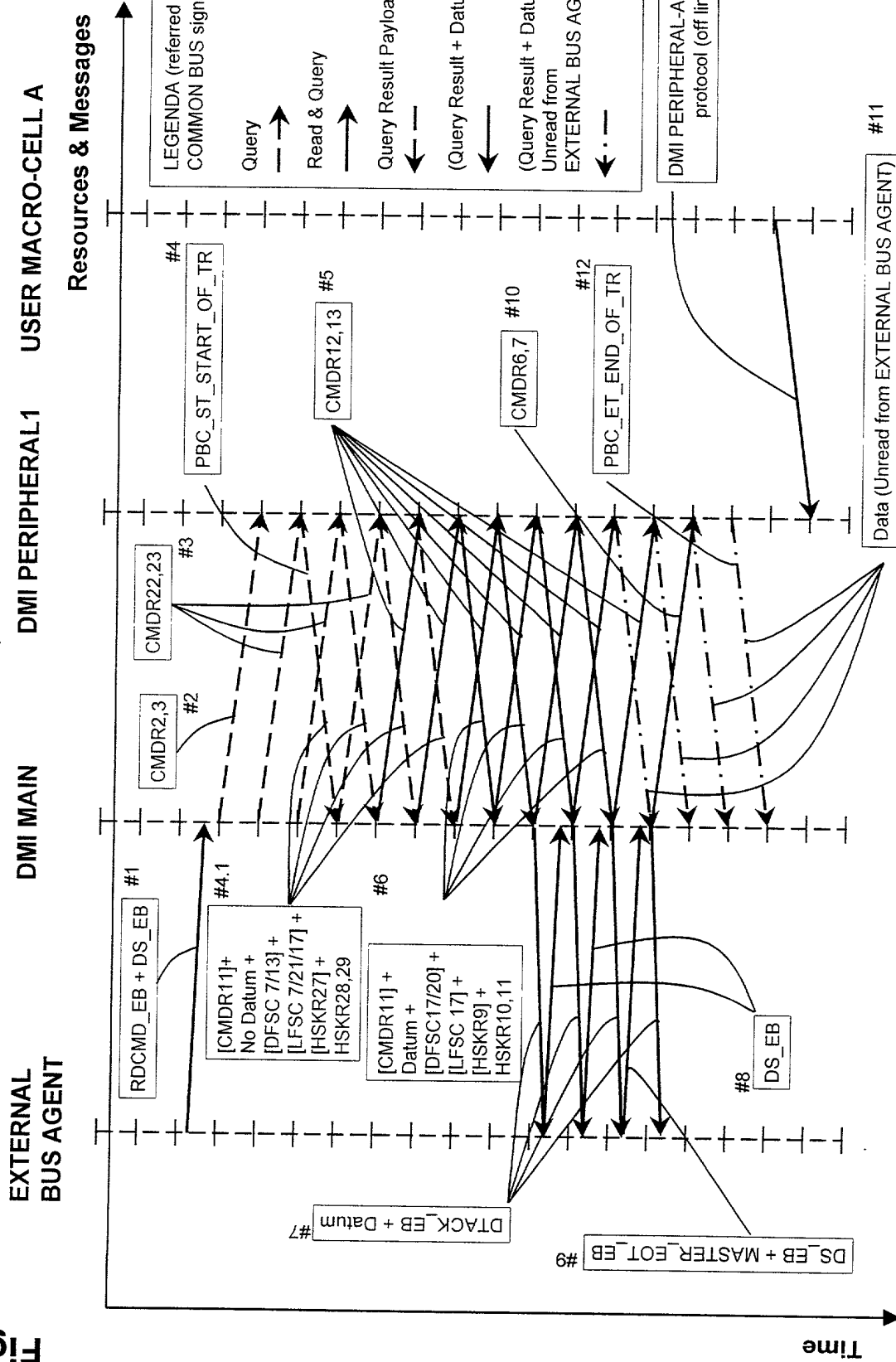


Figure 37

Message Sequence Chart

EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
Burst READ Transaction from DMI PERIPHERAL 1/ Prefetchable resource  
DMI (slave) Termination

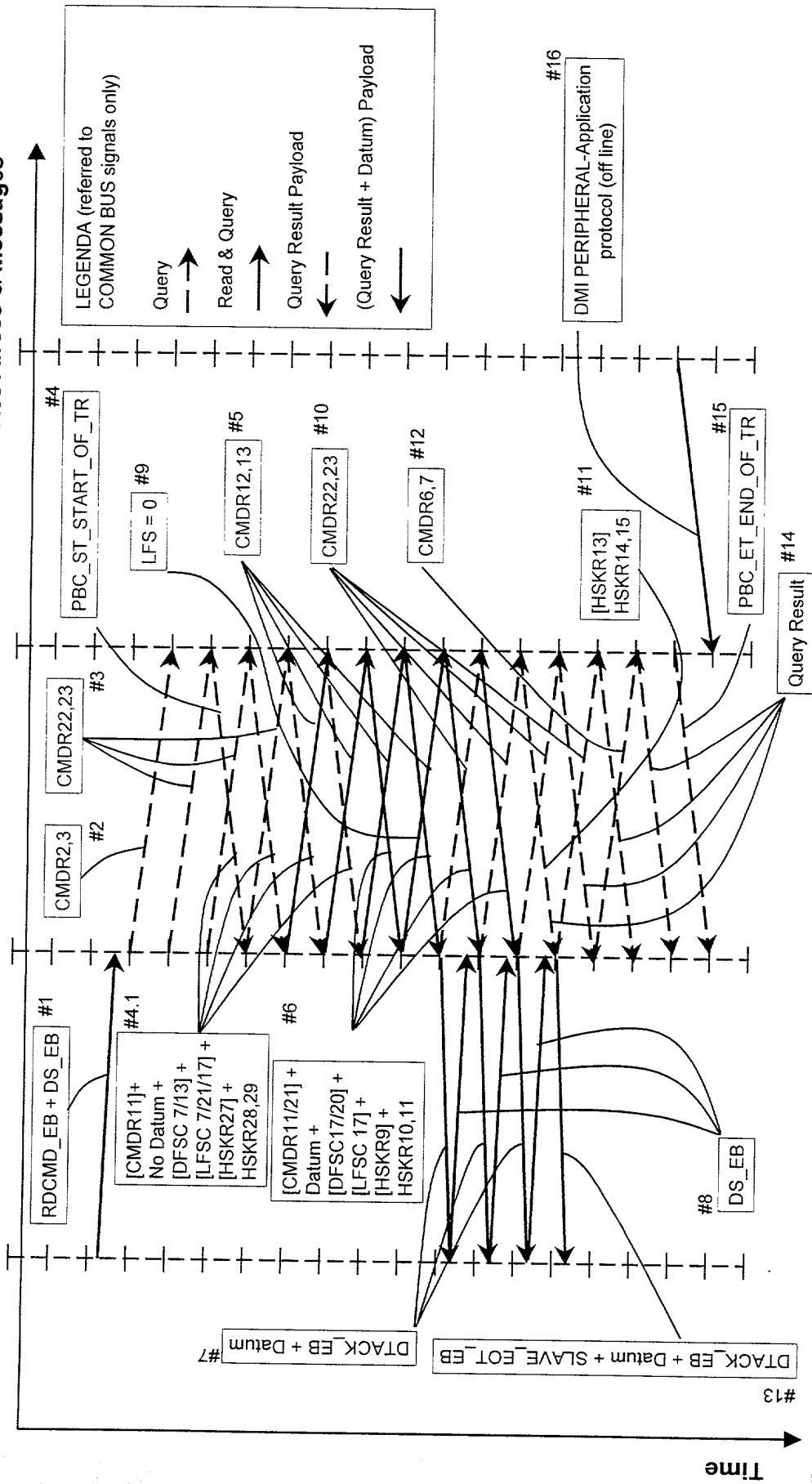
EXTERNAL  
BUS AGENT

DMI MAIN

DMI PERIPHERAL 1

USER MACRO-CELL A

Resources & Messages



# DMI Slave Mode Overall Algorithm Representation Write Transaction from EXTERNAL BUS AGENT + Write Transaction to DMI PERIPHERAL

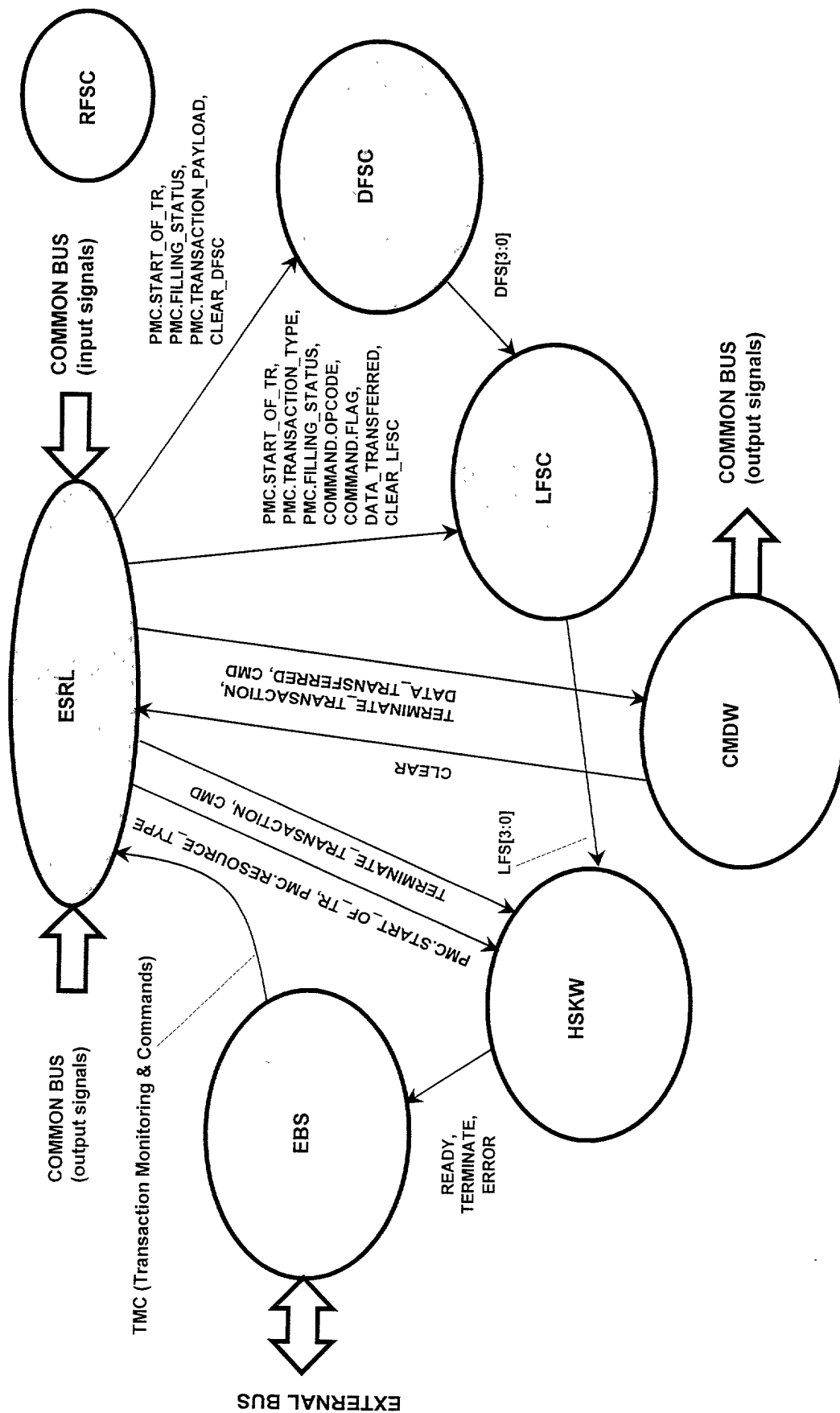


Figure 38

Figure 39

Message Sequence Chart

EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
 WRITE Transaction to DMI PERIPHERAL1/Prefetchable resource  
 EXTERNAL BUS AGENT (master) Termination

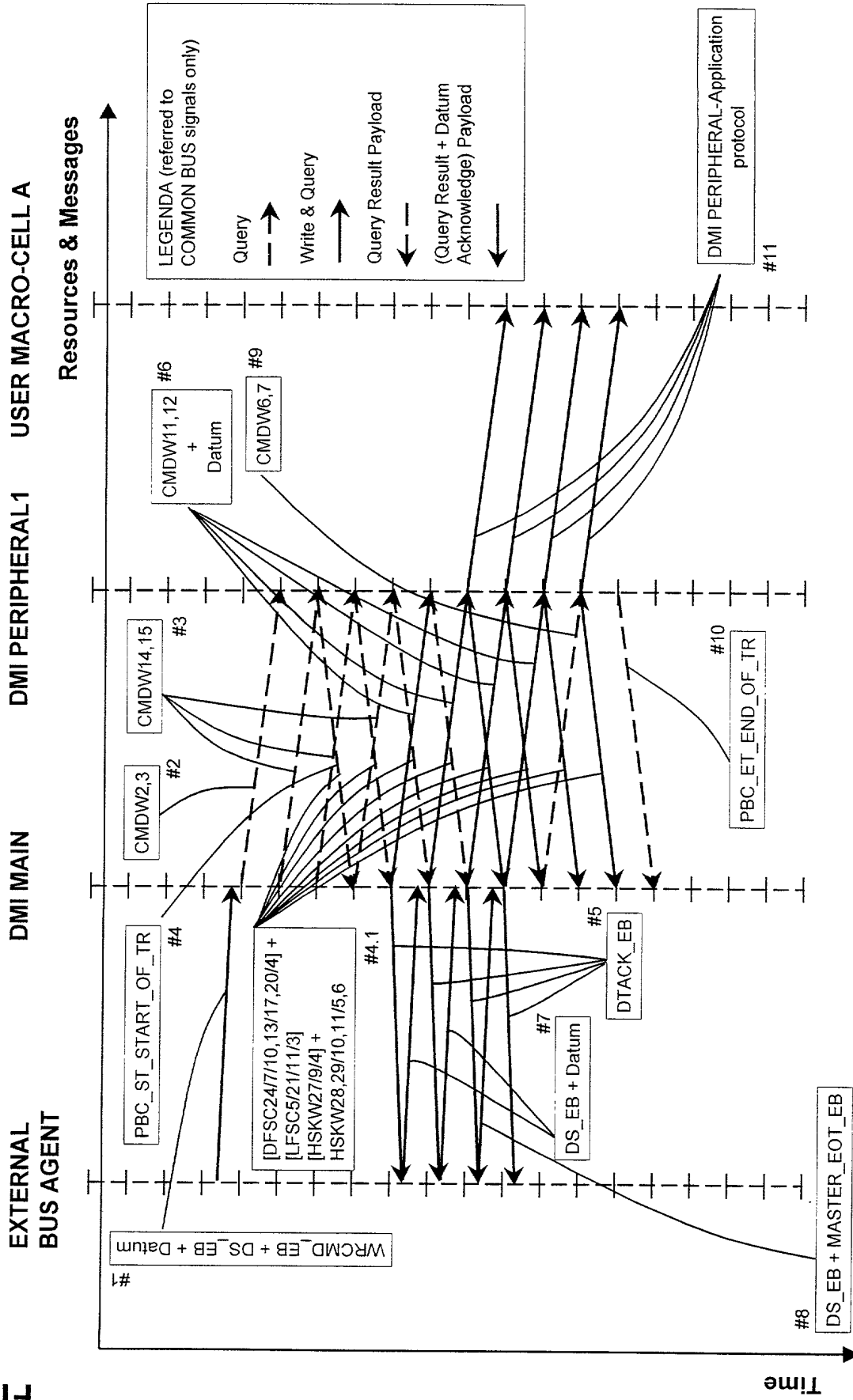
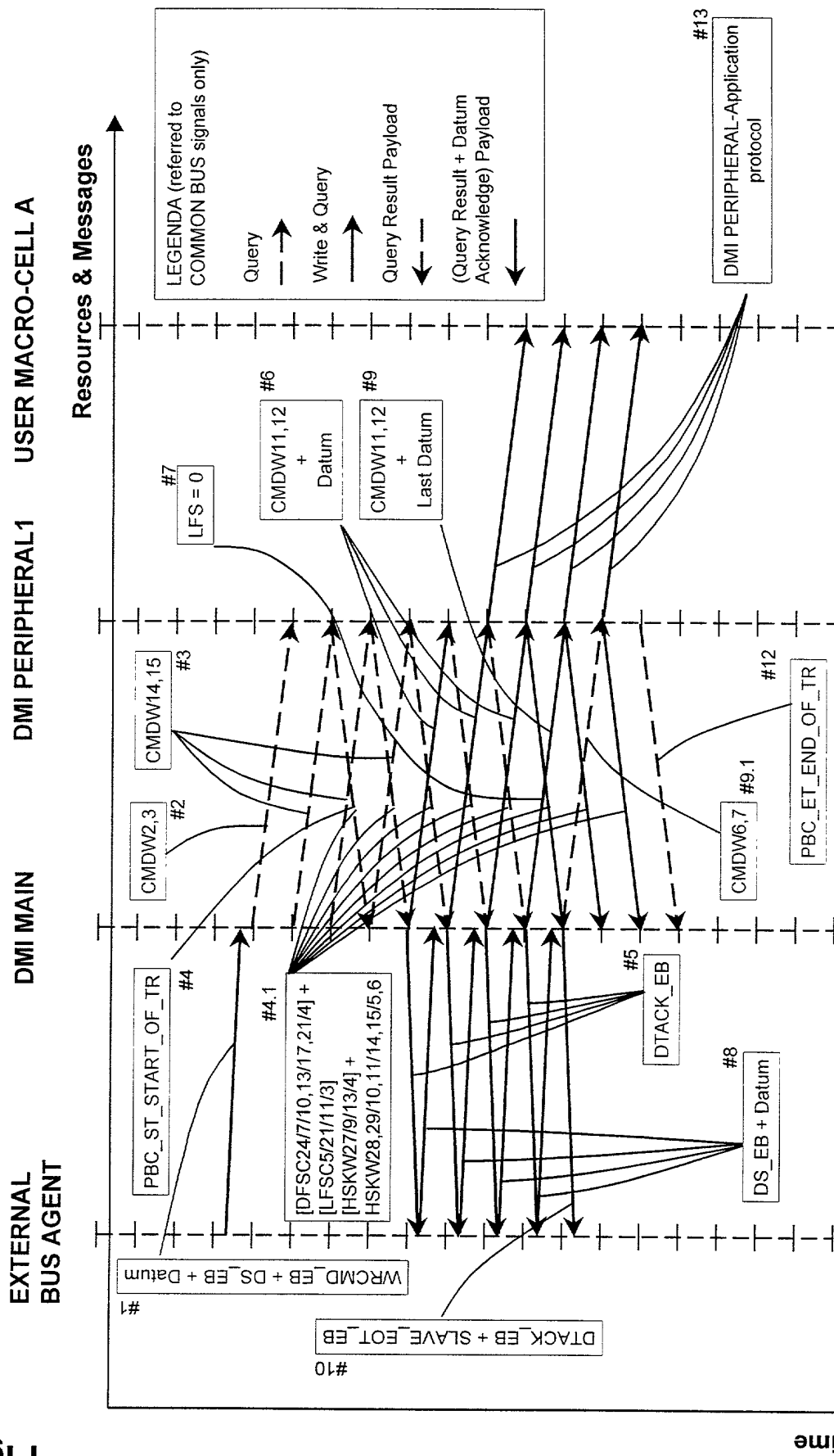


Figure 40

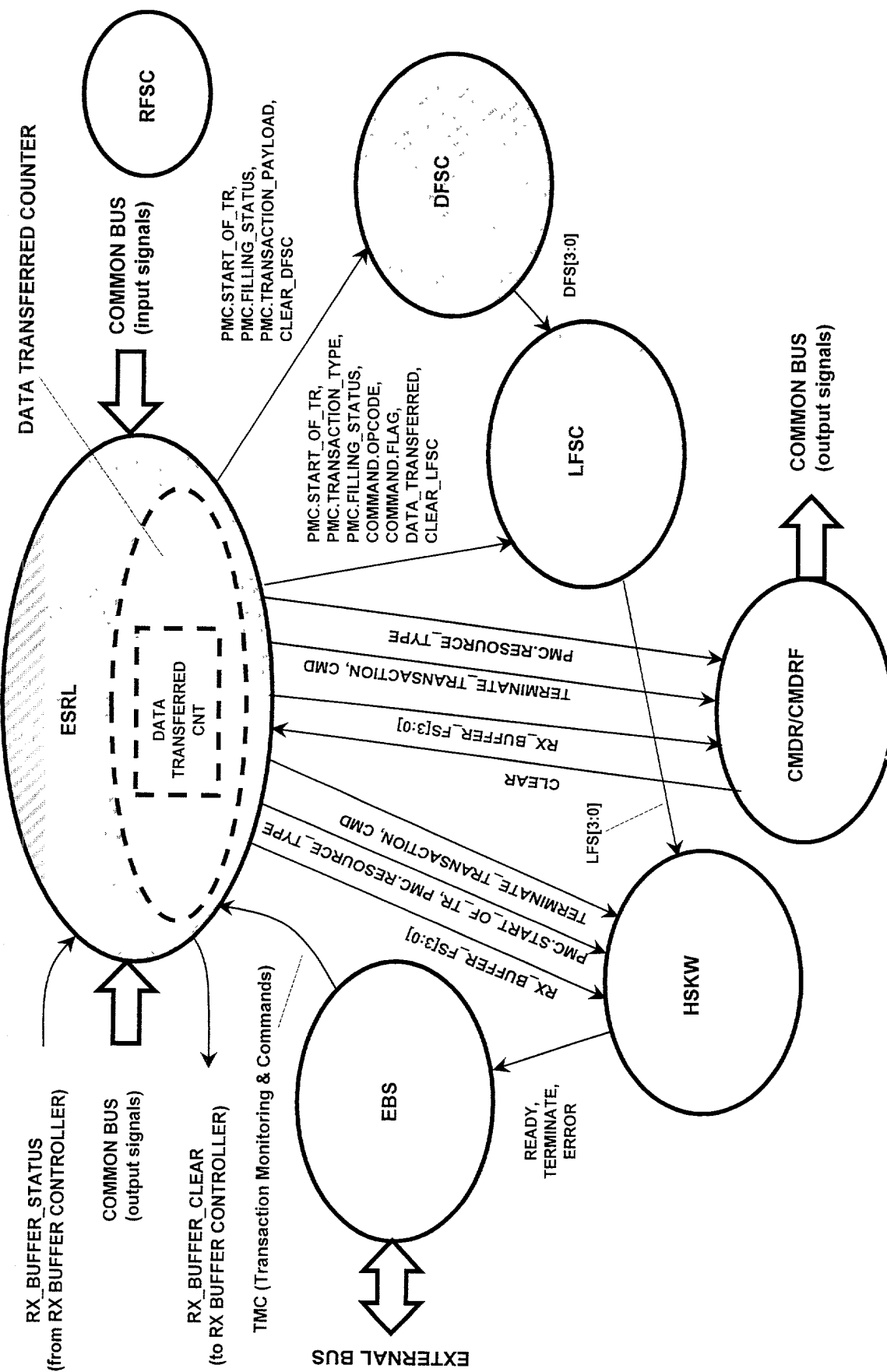
Message Sequence Chart  
 EXTERNAL BUS AGENT acting as Master - DMI acting as Slave  
 WRITE Transaction to DMI PERIPHERAL1/ Prefetchable resource  
 DMI (slave) Termination





**Figure 41**

# DMI Master Mode Overall Algorithm Representation



**PREFETCHABLE FIFO**

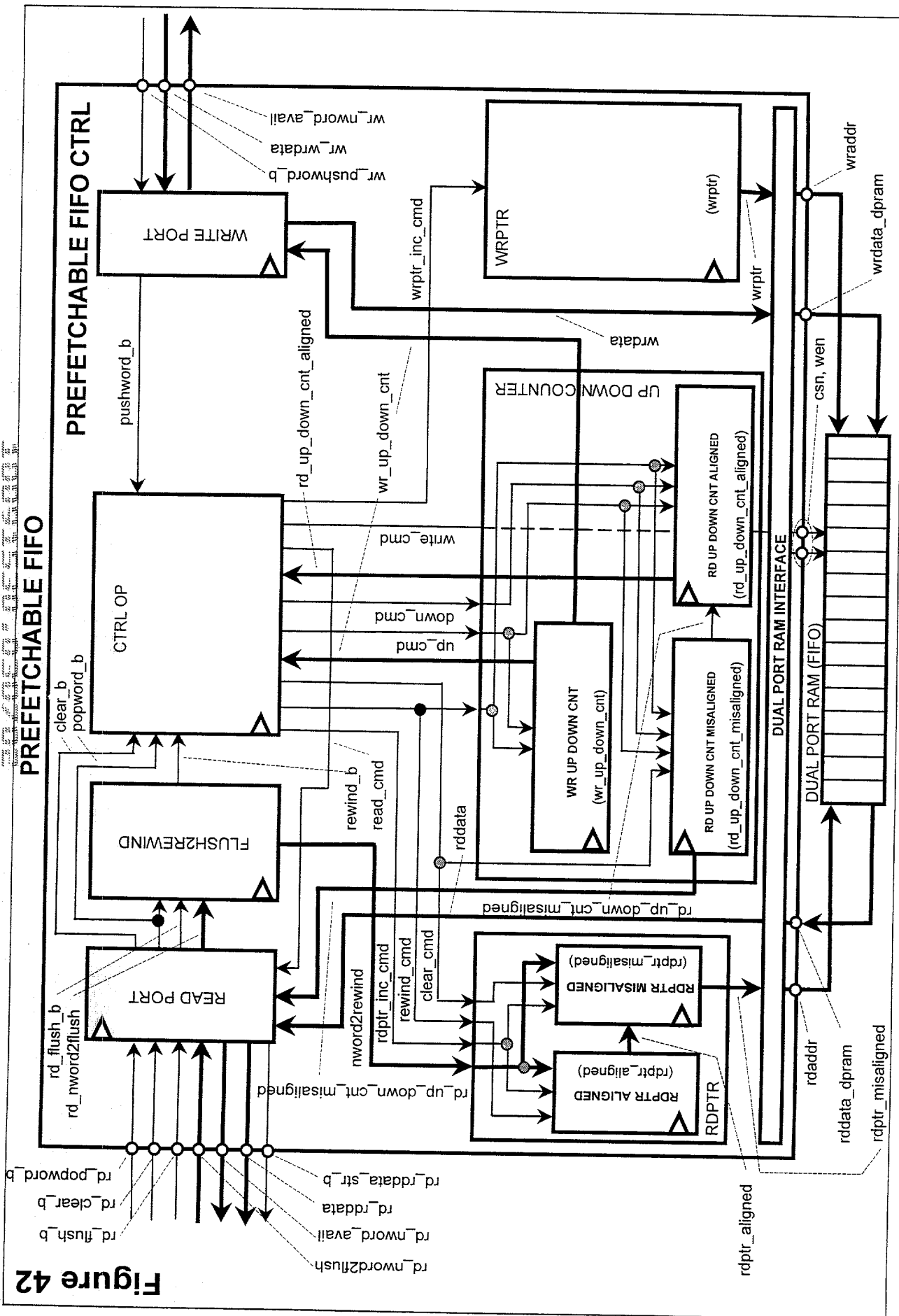


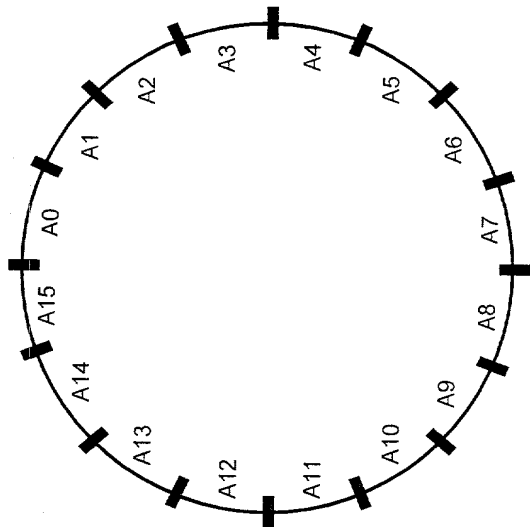
Figure 43

# OVERALL STATUS

SNAPSHOT NUMBER = SN0;  
 BUS STATUS = IDLE;  
 FIFO FS = FIFO EMPTY;  
 DATA\_TRANSFERRED\_CNT = 0;

## ISSUED / EXECUTED COMMANDS

## PREFETCHABLE FIFO STATUS



## UP DOWN COUNTER

wr\_up\_down\_cnt = 0;  
 rd\_up\_down\_cnt\_misaligned = 0;  
 rd\_up\_down\_cnt\_aligned = 0;

## RDPTR

rdptr\_aligned = A0;  
 rdptr\_misaligned = A0;

## WRPTR

wrptr = A0;

## FILLING STATUS

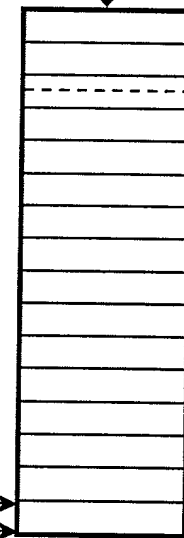
rd\_nword\_avail = 0;  
 wr\_nword\_avail = 16;

## FLUSH2REWIND

rd\_flush\_b = 1;  
 rd\_clear\_b = 1;  
 rd\_nword2flush = 0;  
 popword\_cnt = 0;  
 nword2rewind = 0;  
 rewind\_b = 1;  
 clear\_b = 1;

rx\_buffer\_wrptr  
 rx\_buffer\_rdp1r

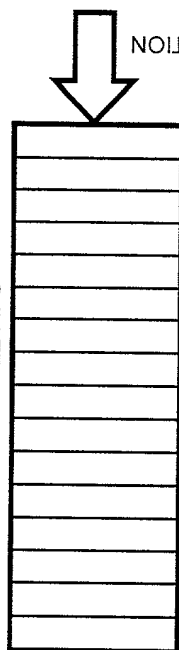
P1



## PARAMETERS

P1 = DATA\_TRANSF\_CNT\_THR = 4  
 P2 = RX\_BUFFER\_FS\_THR = 14

## PREFETCHABLE FIFO



Data-Bus\_leaf2root[31:0]

## PREFETCHABLE FIFO

## POINTERS

ptr1 = rdptr\_aligned  
 ptr2 = rdptr\_misaligned  
 ptr3 = wrptr

Figure 44

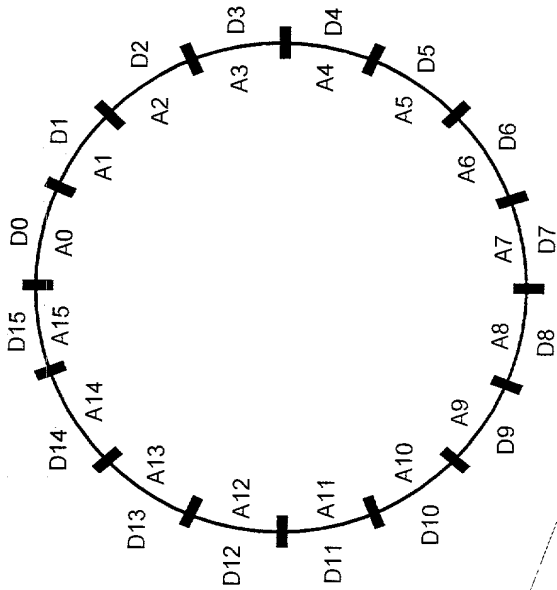
# OVERALL STATUS

SNAPSHOT NUMBER = SN1;  
 BUS STATUS = WORKING;  
 FIFO FS = FIFO FULL;  
 DATA\_TRANSFERRED\_CNT = 0;

## ISSUED / EXECUTED COMMANDS

16 FIFO PUSH EXECUTED;

## PREFETCHABLE FIFO STATUS



## UP DOWN COUNTER

wr\_up\_down\_cnt = 16;  
 rd\_up\_down\_cnt\_misaligned = 16;  
 rd\_up\_down\_cnt\_aligned = 16;

## RDPTR

rdptr\_aligned = A0;  
 rdptr\_misaligned = A0;  
 wrptr = A0  
 (one turn completed);

## FILLING STATUS

rd\_nword\_avail = 16;  
 wr\_nword\_avail = 0;

## FLUSH2REWIND

rd\_flush\_b = 1;  
 rd\_clear\_b = 1;  
 rd\_nword2flush = 0;  
 popword\_cnt = 0;  
 nword2rewind = 0;  
 rewind\_b = 1;  
 clear\_b = 1;

rx\_buffer\_wrptr  
 rx\_buffer\_rdptr

P1

EXTERNAL BUS  
 to

## PARAMETERS

P1 = DATA\_TRANSF\_CNT\_THR = 4  
 P2 = RX\_BUFFER\_FS\_THR = 14

## RX\_BUFFER

P2

Data-Bus\_leaf2root[31:0]

## PREFETCHABLE FIFO

POINTERS  
 ptr1 = rdptr\_aligned  
 ptr2 = rdptr\_misaligned  
 ptr3 = wrptr

## PREFETCHABLE FIFO

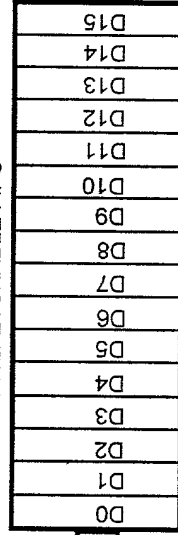


Figure 45

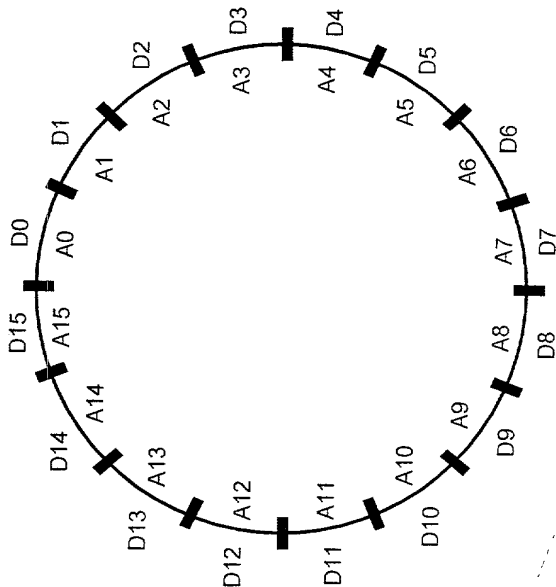
# OVERALL STATUS

SNAPSHOT NUMBER = SN2;  
 BUS STATUS = WORKING;  
 FIFO FS = FIFO FULL;  
 DATA\_TRANSFERRED\_CNT = 0;

# ISSUED / EXECUTED COMMANDS

7 POP EXECUTED;

# PREFETCHABLE FIFO STATUS



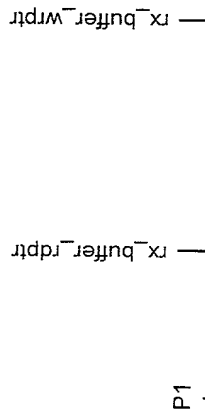
**UP DOWN COUNTER**  
 wr\_up\_down\_cnt = 16;  
 rd\_up\_down\_cnt\_misaligned = 9;  
 rd\_up\_down\_cnt\_aligned = 9;

**RDPTR**  
 rdptr\_aligned = A7;  
 rdptr\_misaligned = A7;

**WRPTR**  
 wrptr = A0;

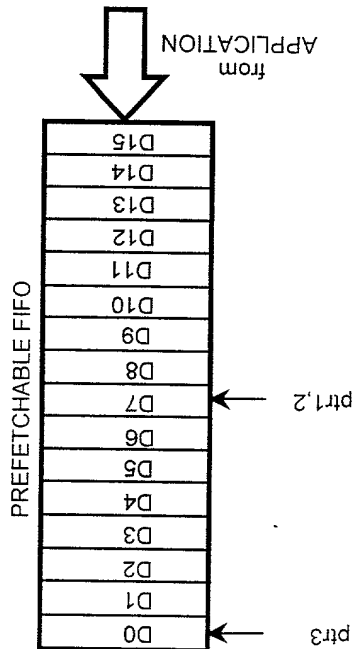
**FILLING\_STATUS**  
 rd\_nword\_avail = 9;  
 wr\_nword\_avail = 0;

**FLUSH2REWIND**  
 rd\_flush\_b = 1;  
 rd\_clear\_b = 1;  
 rd\_nword2flush = 0;  
 popword\_cnt = 7;  
 nword2rewind = 0;  
 rewind\_b = 1;  
 clear\_b = 1;



# PARAMETERS

P1 = DATA\_TRANSF\_CNT\_THR = 4  
 P2 = RX\_BUFFER\_FS\_THR = 14



**PREFETCHABLE FIFO POINTERS**  
 ptr1 = rdptr\_aligned  
 ptr2 = rdptr\_misaligned  
 ptr3 = wrptr

Data-Bus\_leaf2root[31:0]

to  
 EXTERNAL BUS

Figure 46

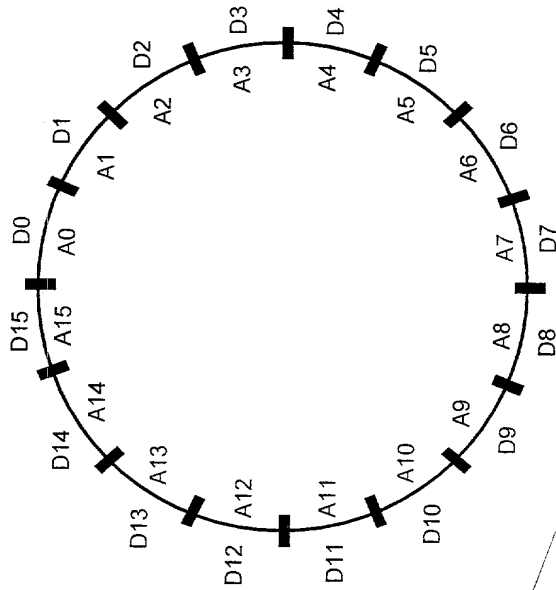
### OVERALL STATUS

SNAPSHOT NUMBER = SN3;  
 BUS STATUS = WORKING;  
 FIFO FS = FIFO FULL;  
 DATA\_TRANSFERRED\_CNT = 4;

### ISSUED / EXECUTED COMMANDS

FLUSH(4) ISSUED;

### PREFETCHABLE FIFO STATUS



### UP DOWN COUNTER

wr\_up\_down\_cnt = 16;  
 rd\_up\_down\_cnt\_misaligned = 9;  
 rd\_up\_down\_cnt\_aligned = 9;

### RDPTR

rdptr\_aligned = A7;  
 rdptr\_misaligned = A7;

### WRPTR

wrptr = A0;

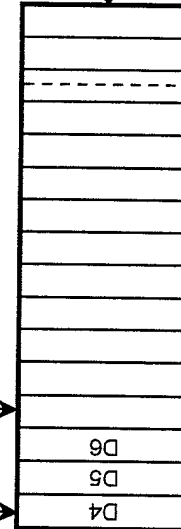
### FILLING STATUS

rd\_nword\_avail = 9;  
 wr\_nword\_avail = 0;

### FLUSH2REWIND

rd\_flush\_b = 1;  
 rd\_clear\_b = 1;  
 rd\_nword2flush = 0;  
 popword\_cnt = 7;  
 nword2rewind = 0;  
 rewind\_b = 1;  
 clear\_b = 1;

rx\_buffer\_wrptr  
 rx\_buffer\_rdptr



### PARAMETERS

P1 = DATA\_TRANSF\_CNT\_THR = 4  
 P2 = RX\_BUFFER\_FS\_THR = 14

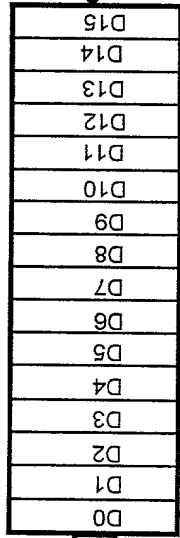
EXTERNAL BUS  
 to

Data-Bus\_leaf2root[31:0]

### PREFETCHABLE FIFO POINTERS

ptr1 = rdptr\_aligned  
 ptr2 = rdptr\_misaligned  
 ptr3 = wrptr

### PREFETCHABLE FIFO



from APPLICATION

Figure 47

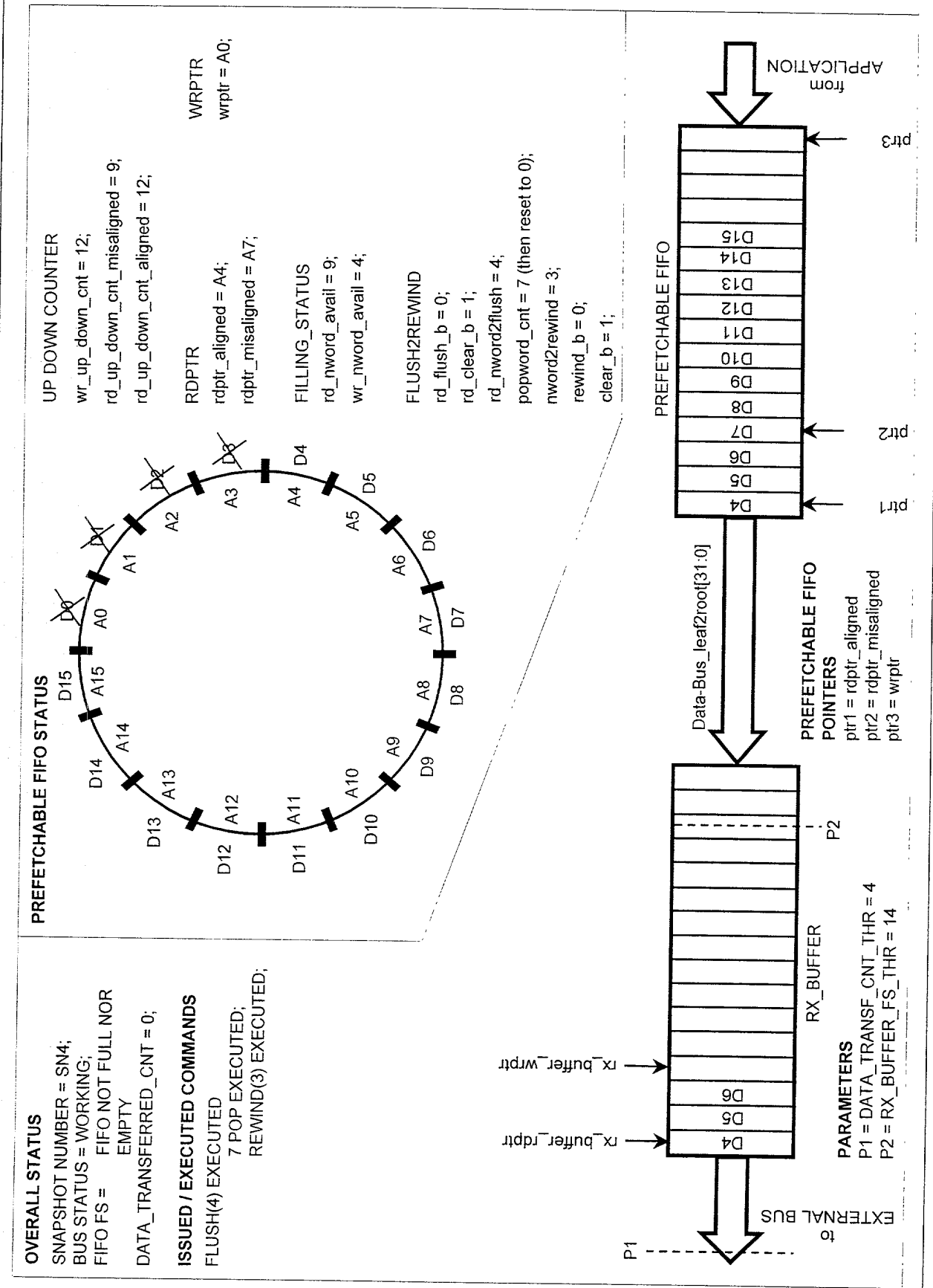


Figure 48

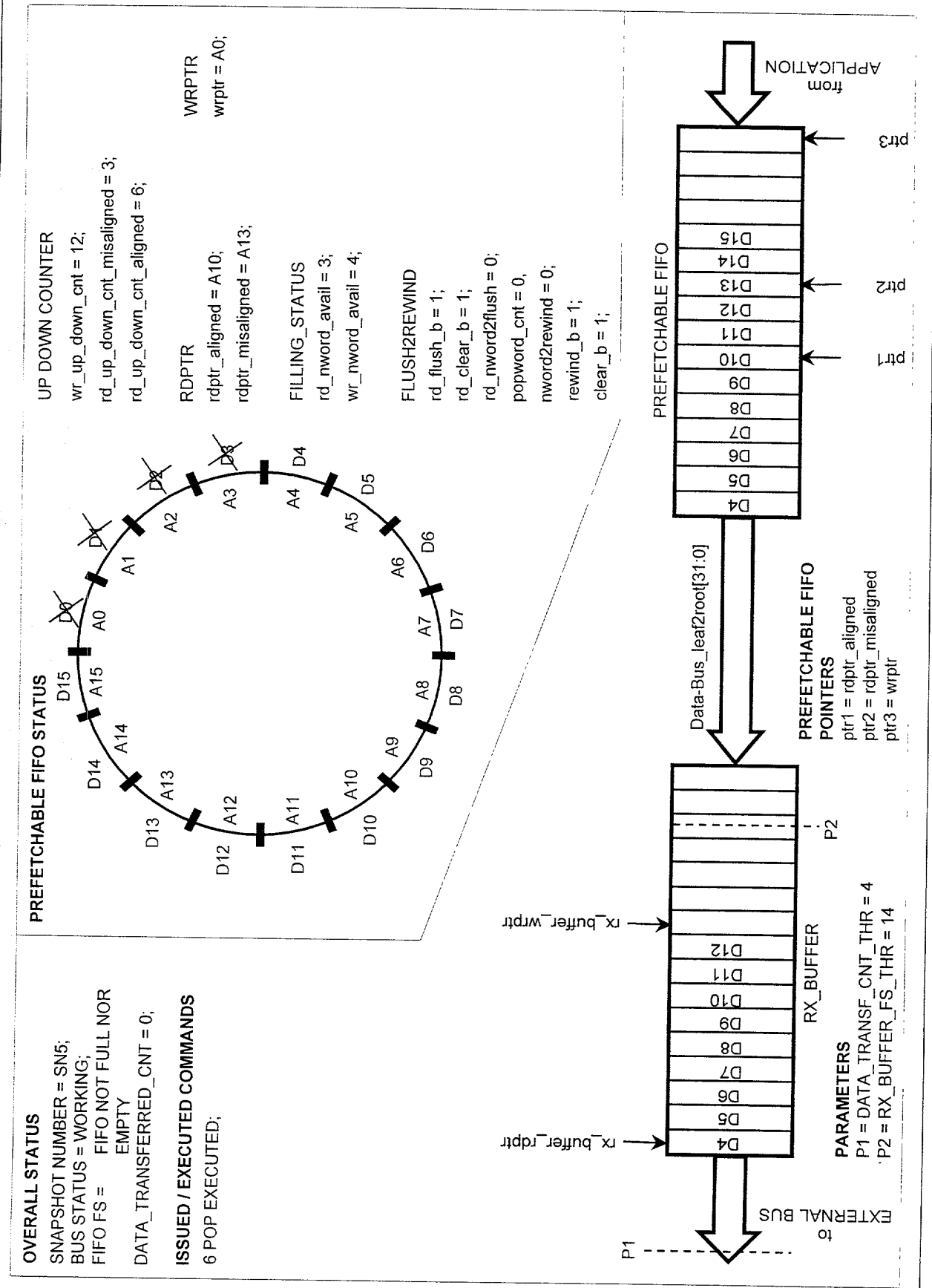




Figure 49

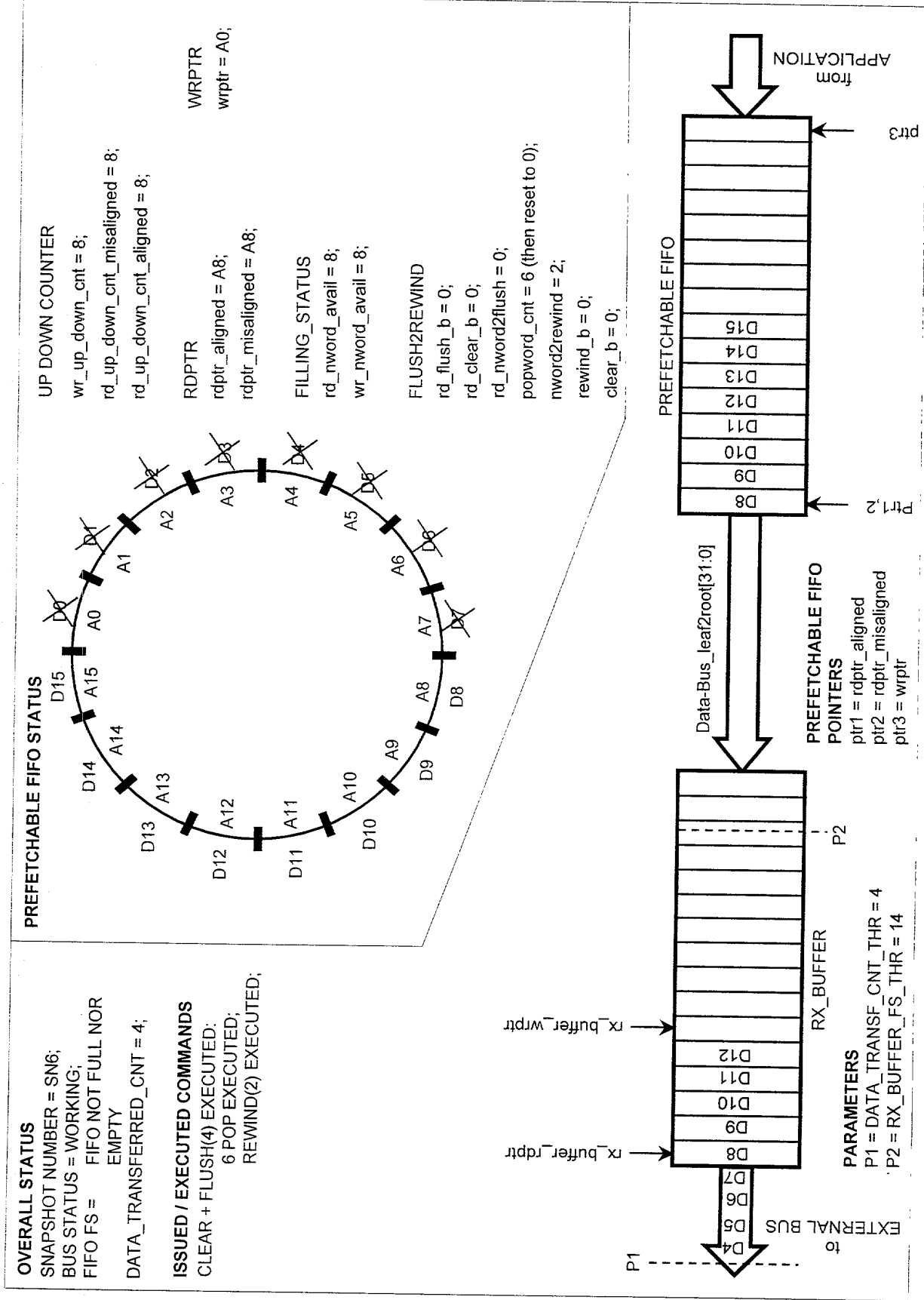


Figure 50

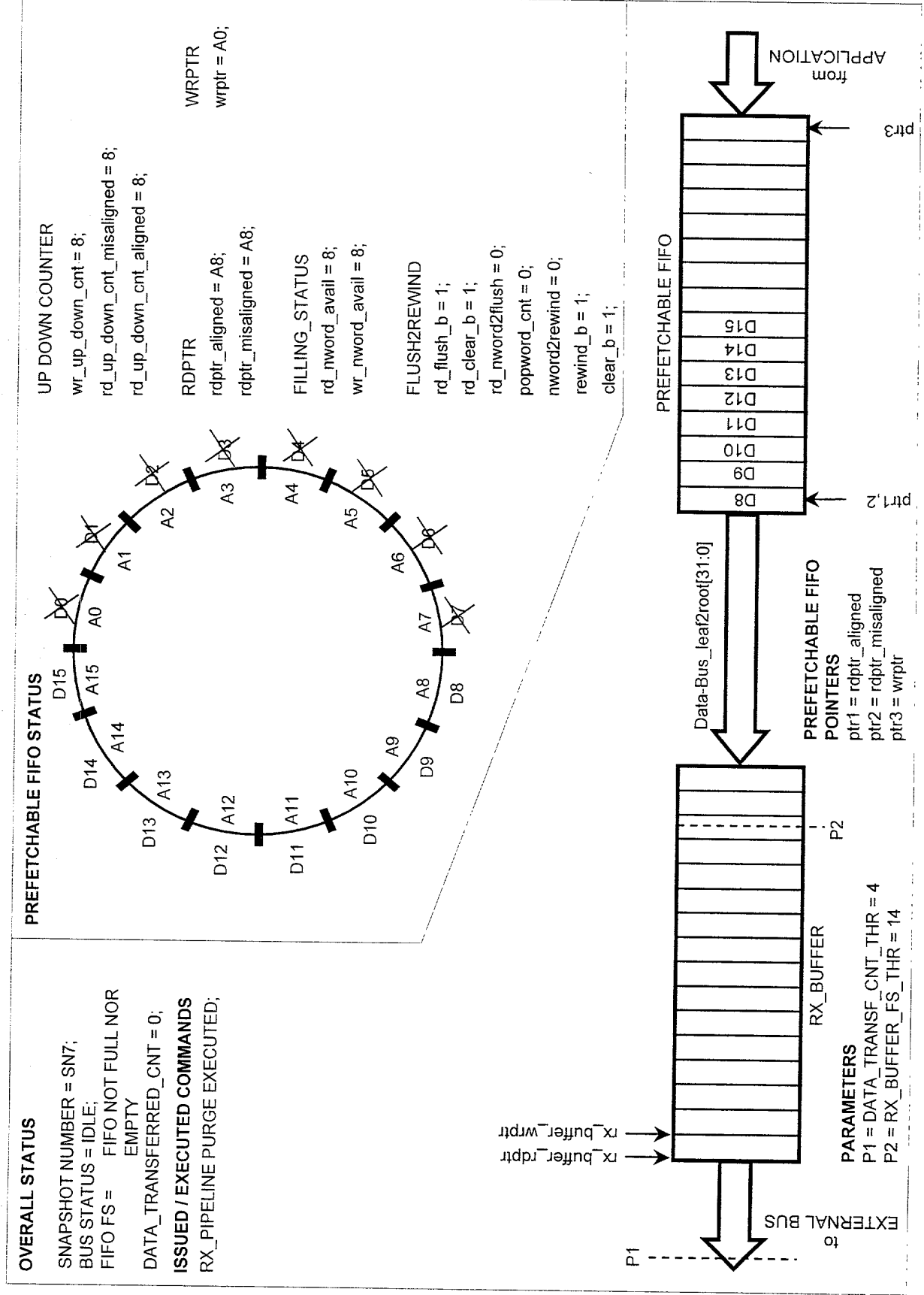


Figure 51

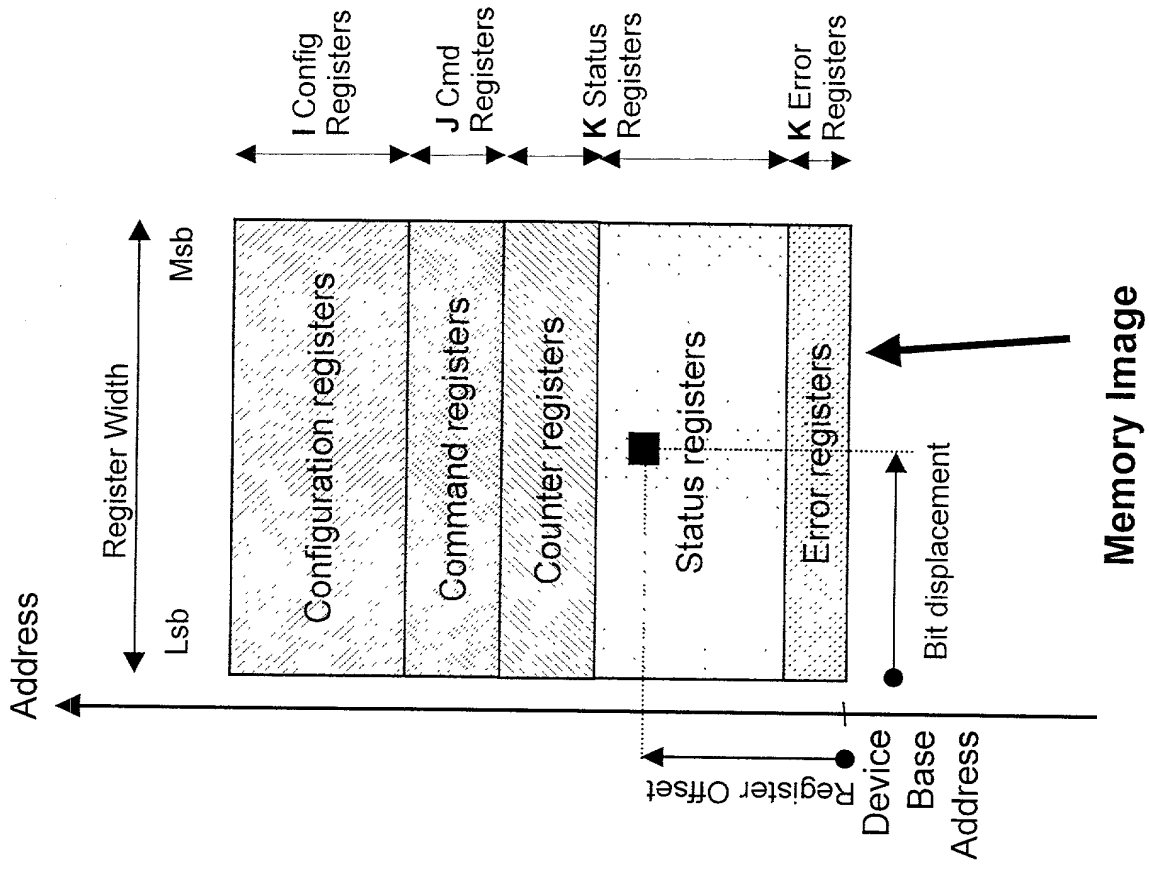


Figure 52

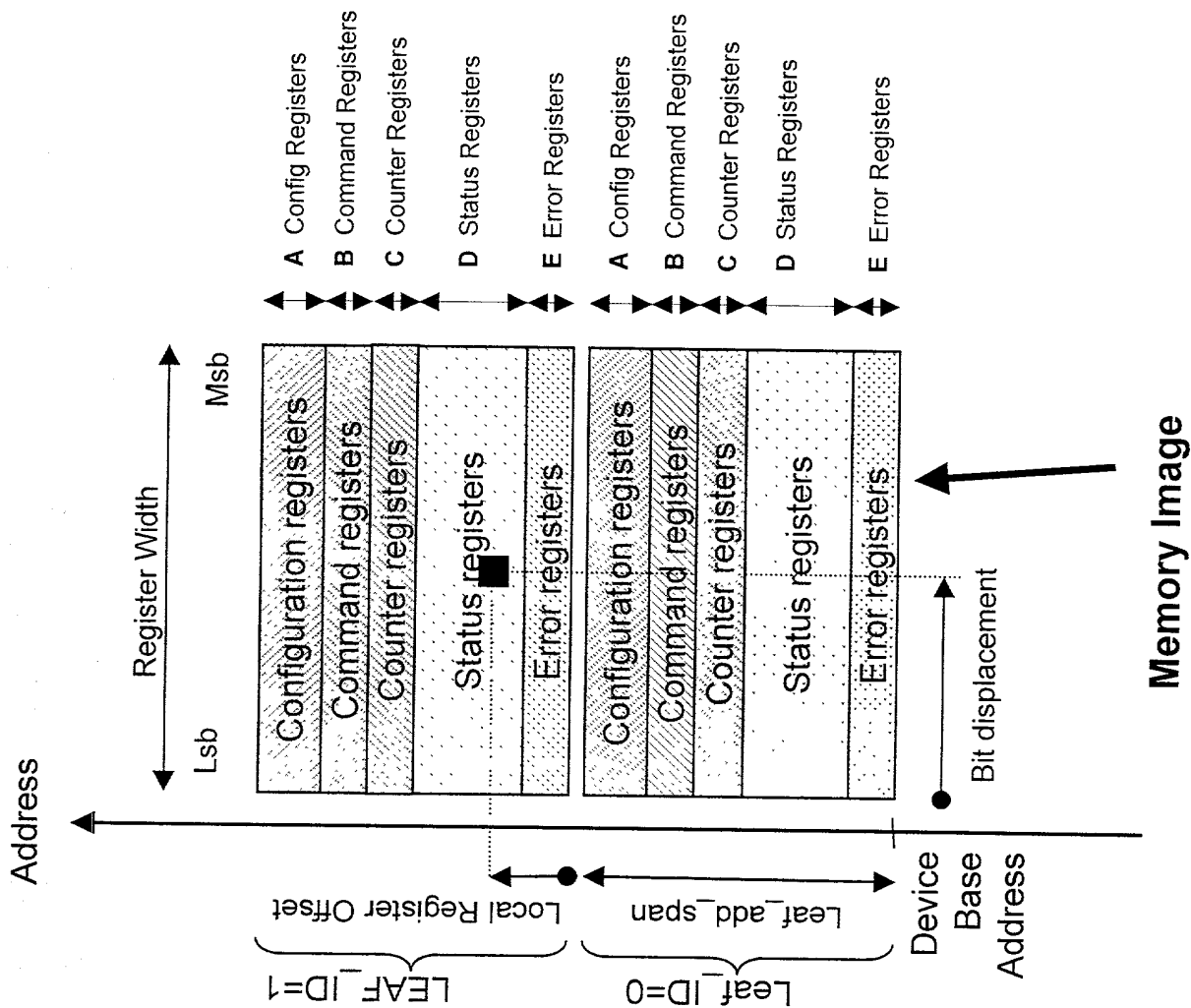


Figure 53

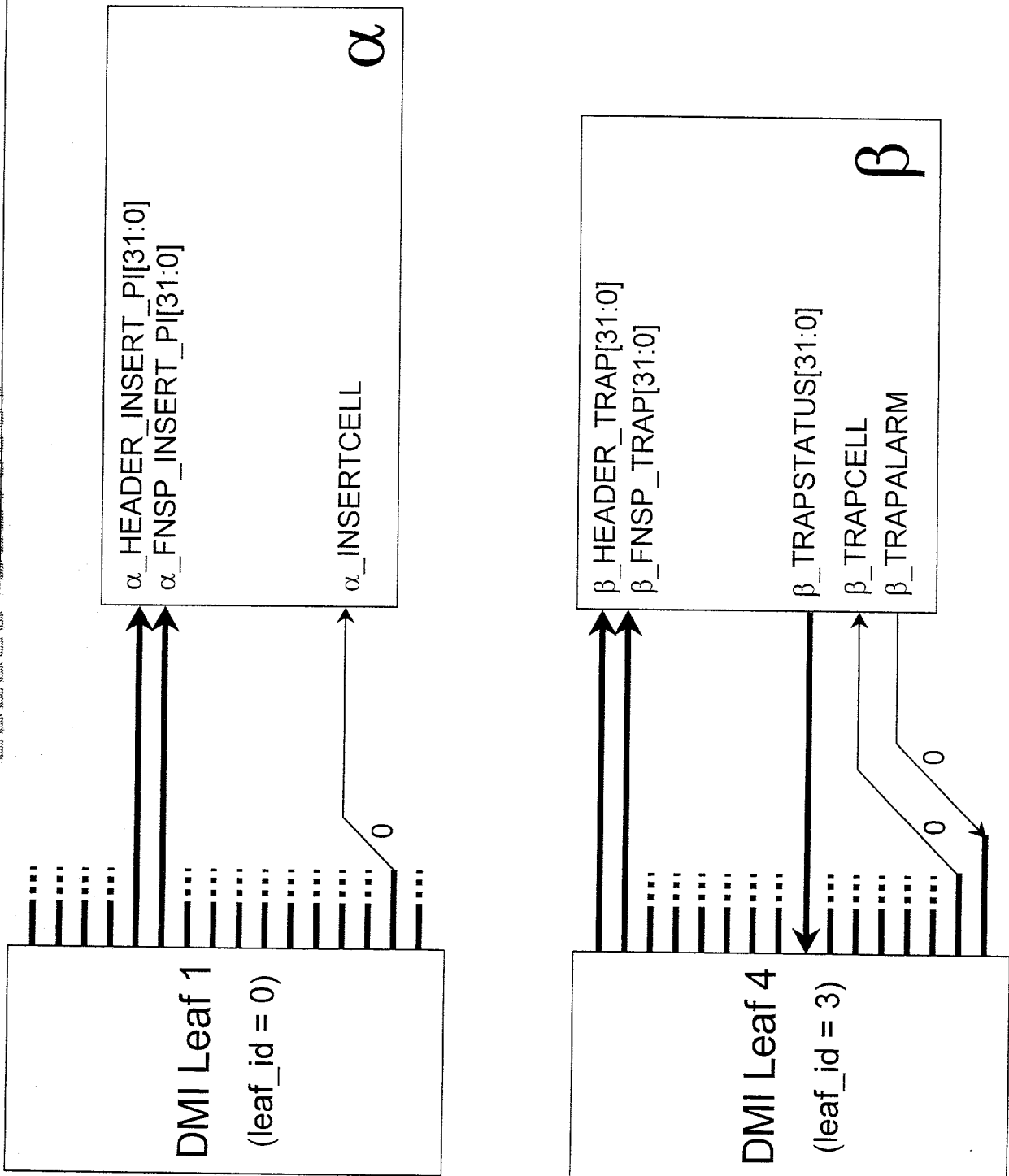
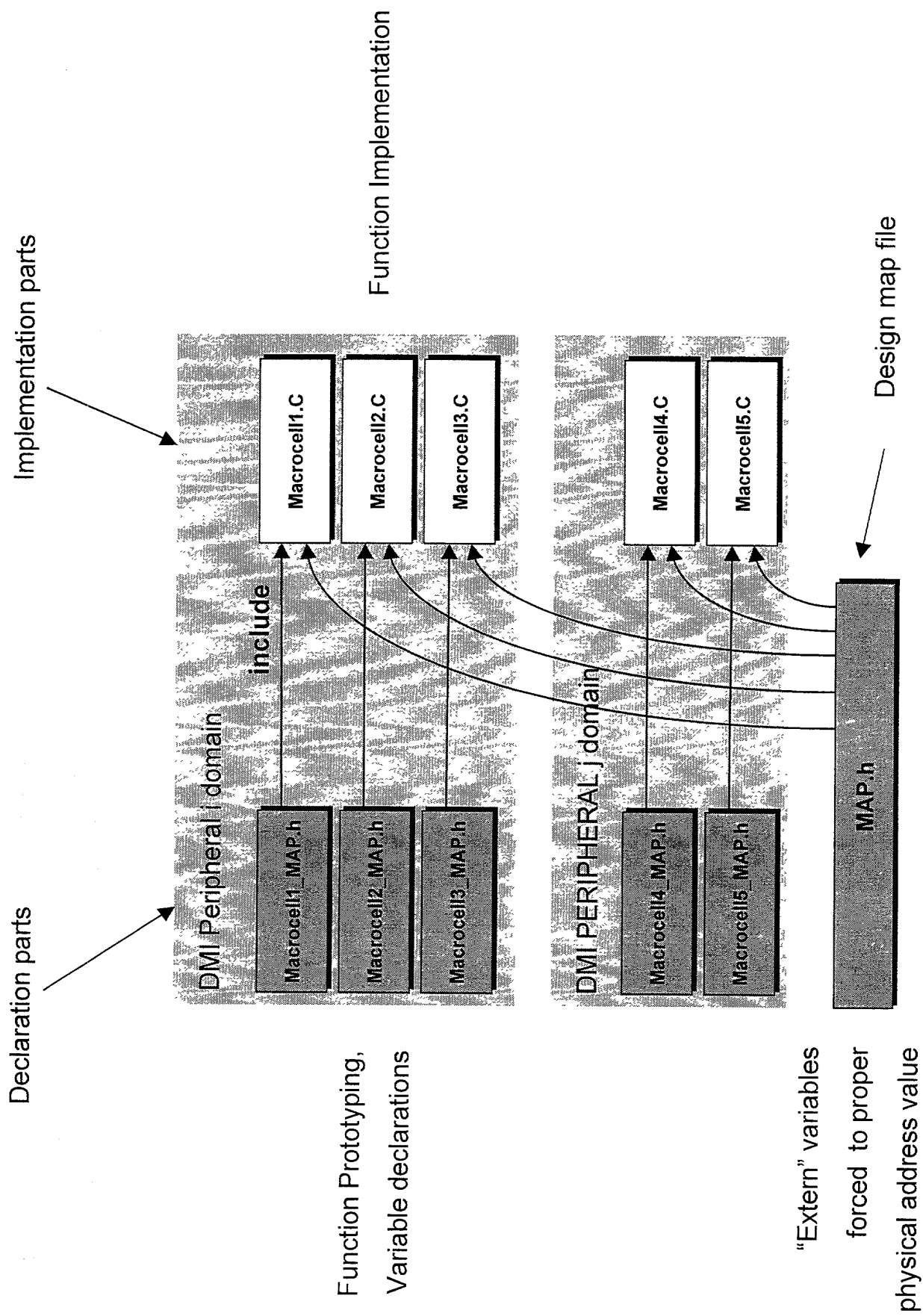


Figure 54



[illegible]

## O.S. Driver Entry Points

